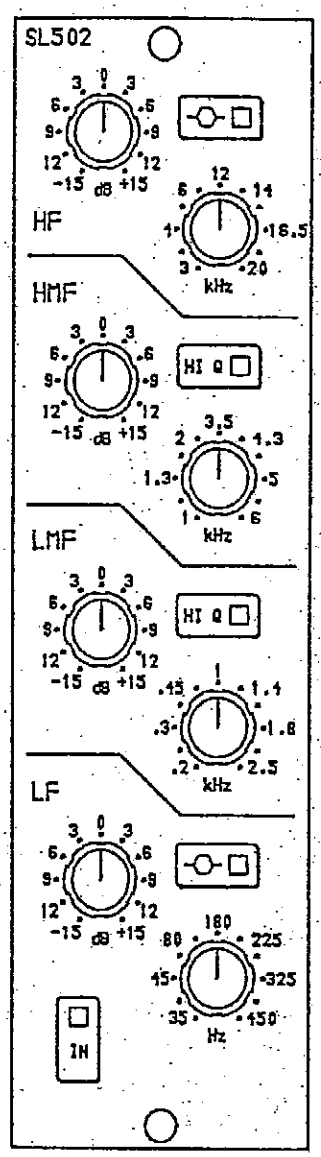
SL 502: MONO FOUR-BAND EQUALISER

1 Front Panel Diagram



2 Operational Description

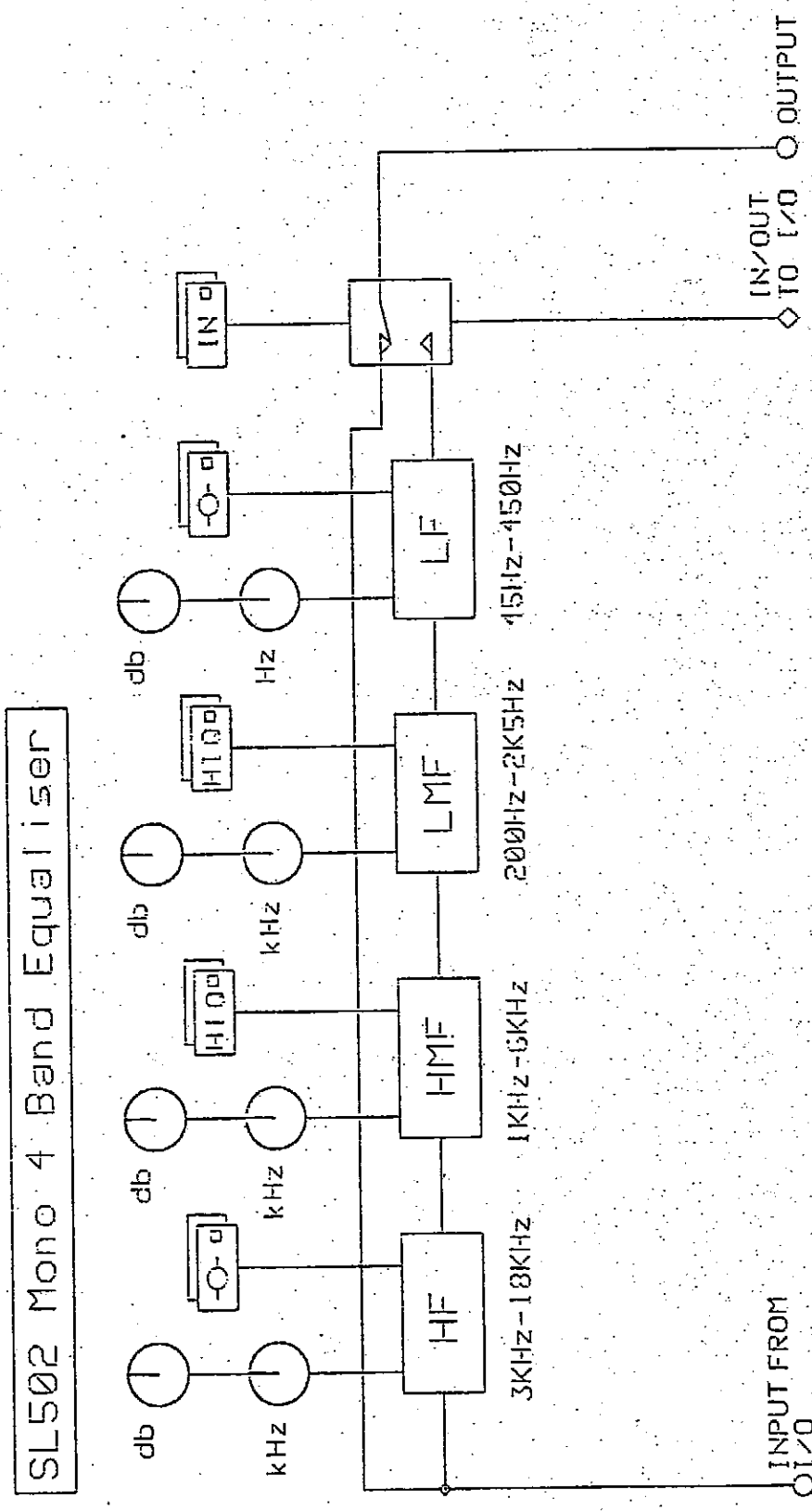
Each band of the SL 502 Mono Parametric Equaliser has a centre-detented rotary gain control with a range of ±15 dB, and a continuously variable frequency control.

The high- and low-frequency bands may individually be switched between shelving and peaking (bell) curves with a Q-value of 1. The Q-values of the two mid-frequency bands may individually be switched to either 1 or 2.5. An overall equaliser IN switch is also fitted.

The frequency ranges of the four bands are:

HF Section:	3 kHz to 20 kHz
HMF Section:	1 kHz to 6 kHz
LMF Section:	200 Hz to 2.5 kHz
LF Section:	35 Hz to 450 Hz

3 Block Diagram



4 Circuit Description

All the front panel switches on this cassette can be controlled by Instant Reset.

The input switching functions so that input to the equaliser is taken from either the channel's send to EQ signal or, if a dynamics cassette is switched into the path, from the dynamics/equaliser intermediate bus. The output of the equaliser is always switched to the channel EQ return bus when EQ IN is selected. This means that if both dynamics and equaliser are switched in, the equaliser is *always* post-dynamics.

The two input FETs, TR16 and TR17, are buffered by IC1. IC2 is an inverting amp working as the summing amplifier for the outputs of the HF and HMF sections; similarly IC7 works in inverting mode as the summing amplifier for the LF and LMF sections. The overall signal path is non-inverting.

There are two filters in the negative feedback paths of each of these summing amps. Each filter consists of two stages: a Wien band-pass inverting filter and an inverting gain-setting stage. Because IC2 and IC7 are inverting, the overall filter path is non-inverting.

The HF BELL switch controls the function of C6 and the positive feedback path of IC3 via R19 and 17. When H5 FET 1 is off, the filter has a high-pass characteristic and the HF boost response is shelving. When this FET is off there is no positive feedback path. When it is turned on, the filter assumes a band-pass characteristic. The positive feedback around IC3 is also operative and so the Q of the filter is increased. This results in a gain increase through IC3 which is compensated for by turning on H5 FET 2 in the feedback path of IC4 thus keeping the overall gain consistent in both SHELF and BELL modes.

Similarly, the LF BELL switch controls the characteristic of the LF filter.

In the HMF and LMF sections, the Q may be switched between 1 and 2.5 by a similar method of changing the amount of positive feedback in the filter stages and then compensating for the change in gain in the following stage so that the overall gain remains constant.

If H17, H18 and associated components are fitted, the equaliser can be used as an external stand-alone unit with electronically balanced input and output. When the equaliser is not switched in, the signal is bypassed through H17 and H18 via TR3.

The current consumption of the cassette is 40 mA.

5 Alignment

The preset potentiometers RV1 and RV2 in the HMF and LMF sections are set at the factory and should need no further adjustment in normal operation. Adjustment of the HMF HI Q preset RV1 is as follows:

1. Turn the HMF ± pot clockwise to full boost.

2. Turn the HMF frequency pot clockwise to the highest possible frequency.

3. Select Low Q (Q of 1).

4. Feed the input with a sine wave oscillator set to 0 dBu output.

5. While monitoring the equaliser output level with an audio level meter, adjust the oscillator frequency until peak output level (+15 dBu) is reached.

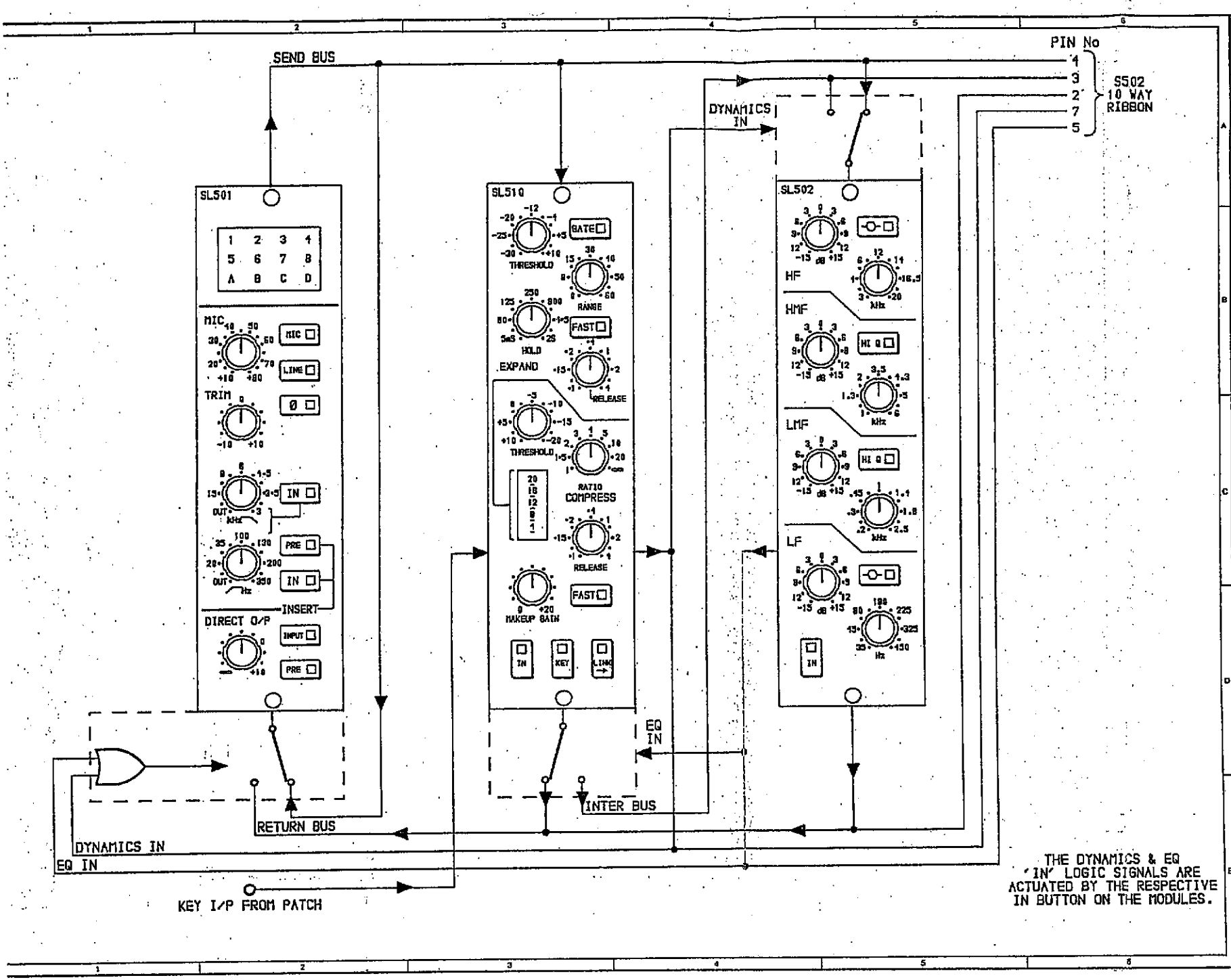
6. Switch to Hi Q, and adjust RV1 so that the amplitude is equal to that achieved in step 5 (±0.1 dB)

Repeat the procedure for the LMF section to adjust RV2.

6 Circuit Diagrams

The following system and circuit diagrams are provided:

System Drawing	T 85010.41	SL 502 – 7
SL 502 Mono Equaliser	T 85002.71	SL 502 – 9
	T 85002.72	SL 502 – 11
	T 85002.73	SL 502 – 13



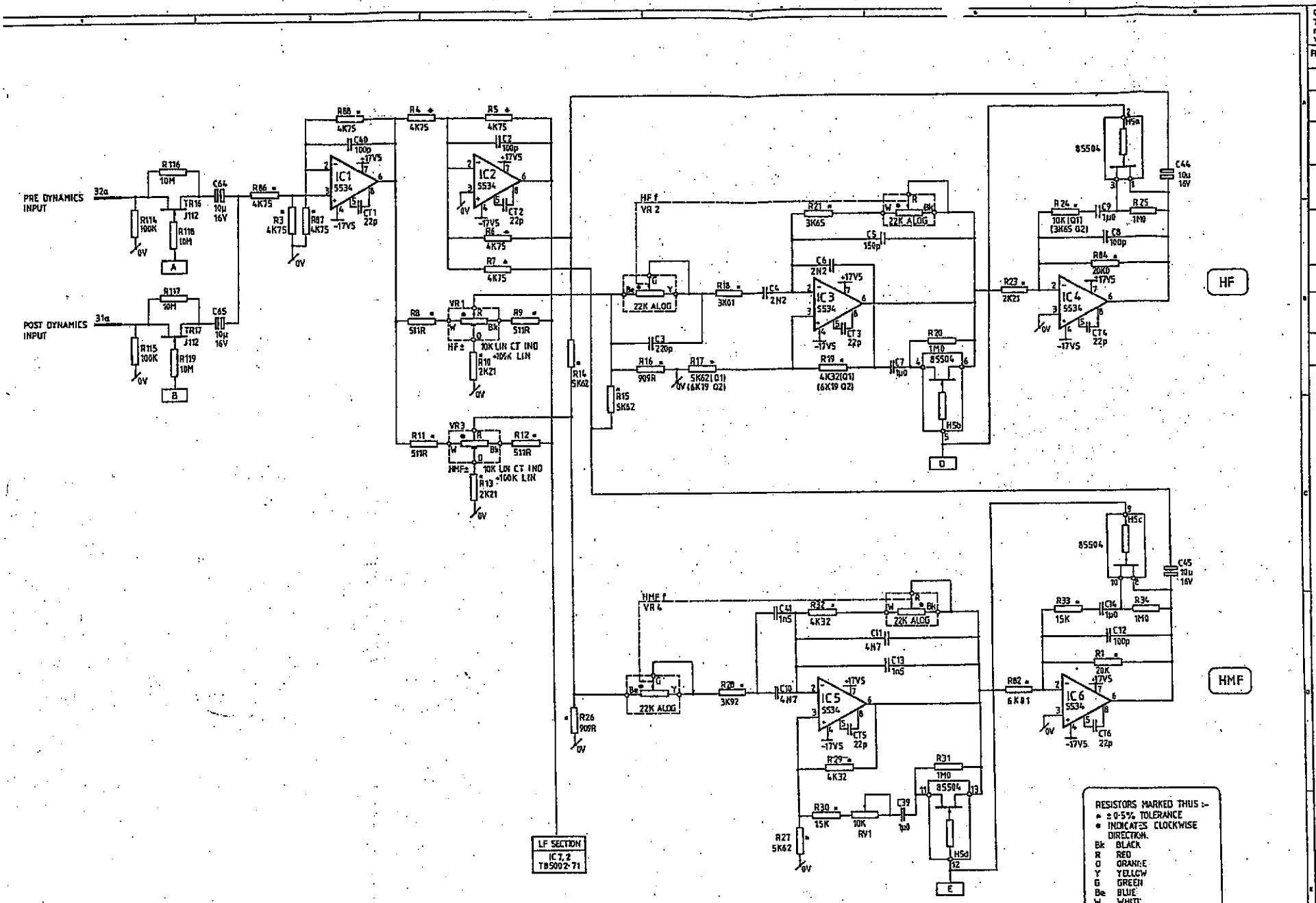
Rev.	Date	Chk'd	Details
A	23 01 87	JEv	NEW DRG. ADDED.

SL500 SHT. 18

Title SL510 MONO DYNAMICS SYSTEM DRAWING.

Drg.No. 53500141

Solid State Logic

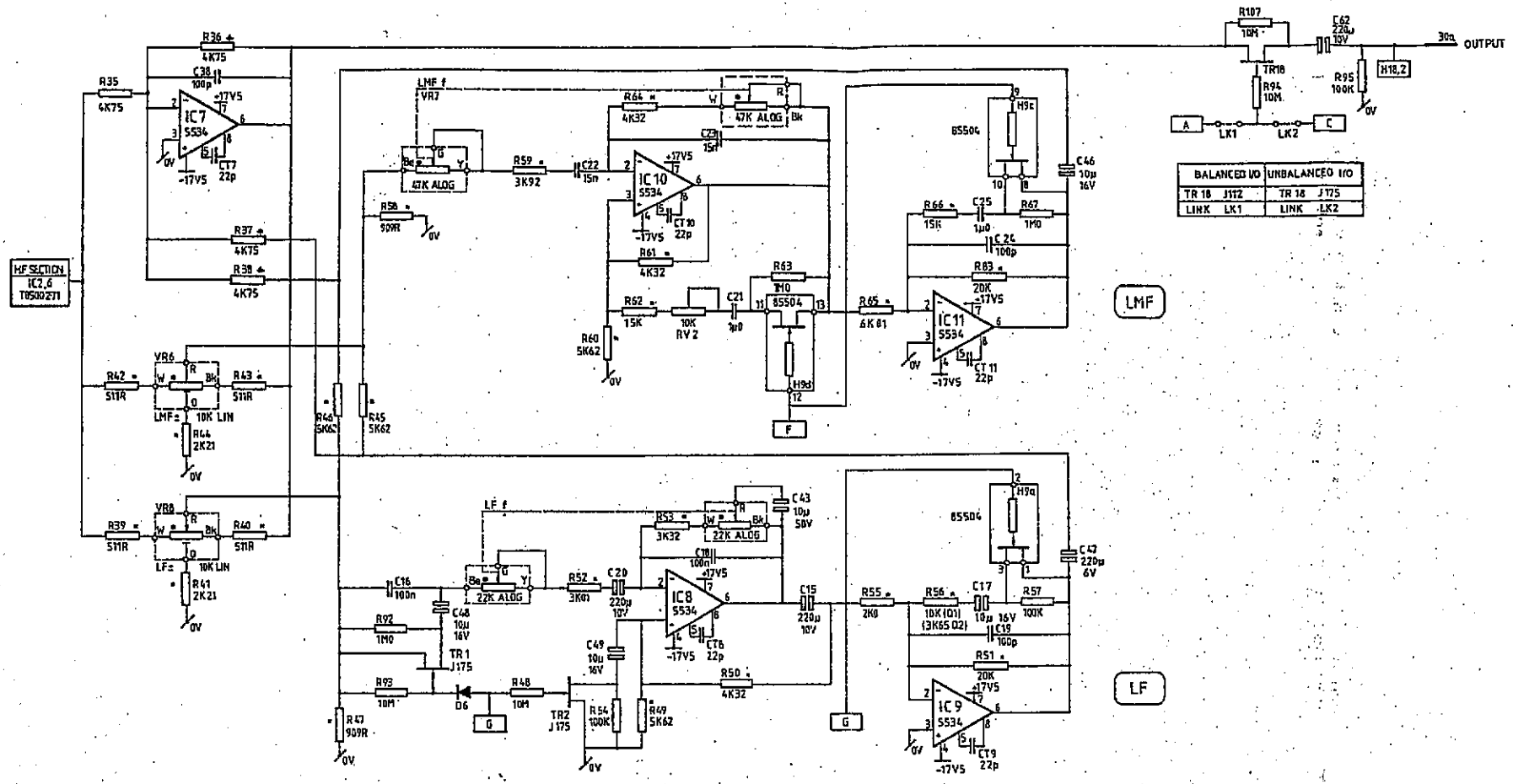


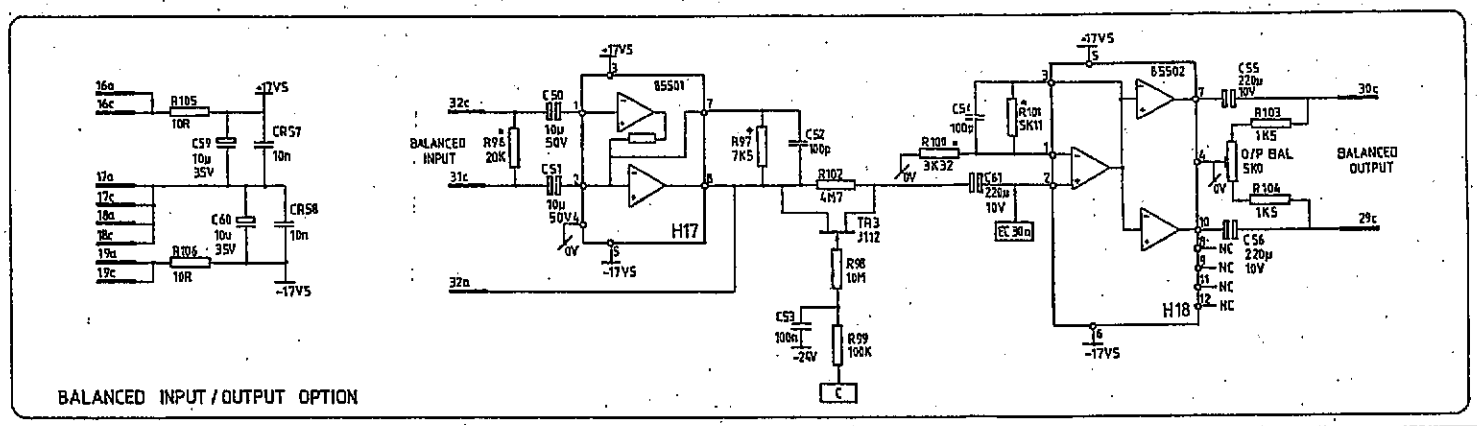
Rev.	Issue	Chkd	Details
0	a	JE May86	NEW DRAWING
0	b	JE July86	R116 & R117 WERE 4M7 NOW 10M. C2 WAS 220p NOW 100p.
1	a	JE Oct86	R8-9 R11-12 WAS 510R NOW 511R. R16-26 WAS 1K8 NOW 909R. C40. 220p ADDED
1	b	Oct 86	R14 & 15 WERE 5K6 NOW 5K62. R82 WAS 6K81 NOW 7K5, PREVIOUS AMENDMENT WAS 0c
1	c	BC Oct 86	C40 WAS 220p NOW 100p C44, 45, 64, 65. 16V ADDED = ADDED TO R 1, 3, 10, 13, 14 R15, 17, 18, 19, 21, 23, 24, 27, 28 R29, 30, 32, 33, 82, 84, 86
1	d	BC Nov86	R82 6K81 WAS R82 7K5
1	e	BC Dec86	C4 & C6 2200p NOW C4 & C6 2N2 > C10 & C11 4007p NOW C10 & C11 4N7
1	f	May 87	LF SECTION NOTE READ TO LF SECTION T85002-72 ONLY.

Title: SL502 MONO EQUALISER.

Drg.No. T85002-71

Solid State Logic





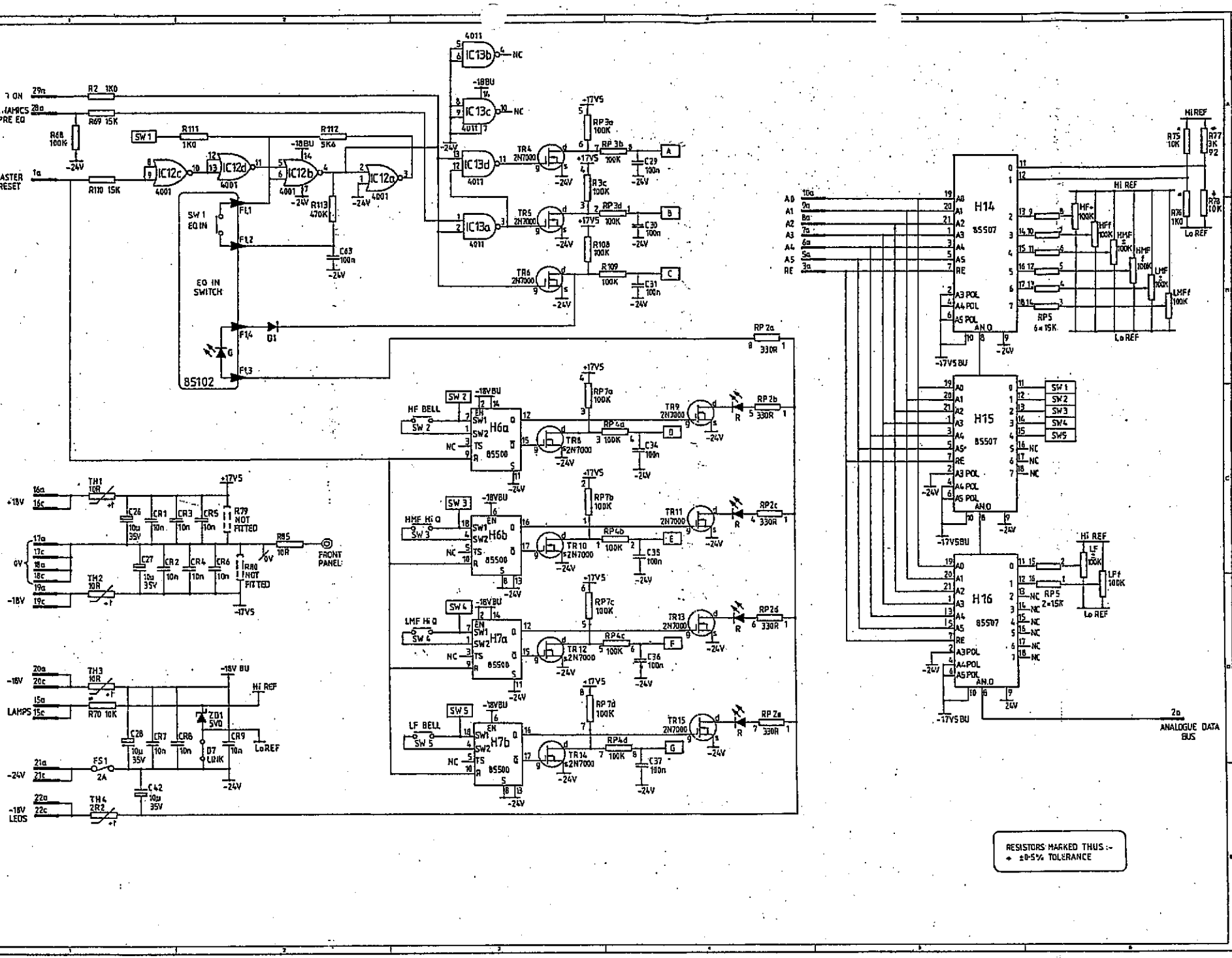
RESISTORS MARKED THUS:-
+ ± 0·5% TOLERANCE
▪ INDICATES CLOCKWISE DIRECTION.
Bk BLACK
R RED
O ORANGE
Y YELLOW
G GREEN
Be BLUE
W WHITE

Rev.	Issue	Chkd	Details
0	a	JE May86	NEW DRAWING
0	b	JE July86	R39-40 & R42-43 WERE 1K0 NOW 510R. R45-46 WERE 12K NOW 5K6 C38 WAS 220p NOW 100p.
1	a	JE Oct 86	R39-40 & R42-43 WAS 510R NOW 511R. VR6:8 WAS 22K LIN NOW 10K LIN. R47:58 WAS 1K8 NOW 909R.
1	b	Oct 86	R45 & 46 WERE 5K6 NOW 5K62. R65 WAS 2K21 NOW 2K0 R65 WAS 6K81 NOW 7K5 PREVIOUS AMENDMENT WAS c.
1	c	BC Oct 86	C43, 50V ADDED C59,60 35V ADDED. C46,48,49,50 C51, 16V ADDED. C15,20 C47,55 61,62 ,10V ADDED ▪ ADDED TO R43,44,49 R50,51,52,53,56,59,60,61 R62, 65, 66, 83, 96, 100, 101
1	d	BC Nov '86	R65 6K81▪ WAS R65 7K5▪ 16V ADDED TO C17 10µ
1	e	BC Dec86	LK1 & LK2 EXCHANGED ON THE TOP NOTE BOX
1	f	May'87	R38 MOVED: HF NOTE MOVED: C47 WAS 10V C50 & 51 WERE 16V WIRE COLOURS ADDED TO PRESET RES. ADJ. TO C101 EL.

Title
SL502
MONO EQUALISER

Drg.No. T85002·72

Solid State Logic



Rev.	Issue	Child	Details
0	a	JE May86	NEW DRAWING
0	b	JE June86	SWT ADDED ADJ R111 & AT 'EQ IN'
0	c	July86 J.E&P	10K ADDED TO R75, 3K92 ADDED TO R76, PINS AMENDED H16 WIRES AMENDED ADJ IC12, R85 ADDED.
0	d	J.E&P Sept86	RP5 ADDED
1	a	Oct86	BOARD REVISION LEVEL UPDATED.
1	b	BC Oct 86	CONN. IC12,11 – R112 AMENDED TO IC12,6 – R112 CONN IC13,1&2 AMENDED, LED COLOURS ADDED. C 26,27,28,42 35V ADDED. FS1, 2A ADDED. RP 5.15K ADDED. *ADDED TO R75 & R76.
1	c	BC Nov86	* ADDED TO R70 10K E.L.
1	d	BC 12.86	R77 10K NOW R77 3K92 : R76 3K92 NOW R76 1K0 : R76 1K0 NOW R78 10K
1	f	May 87	RP2 PIN NUMBERS ADDED : RP2e MOVED : RP5 PIN NUMBERS ADDED : R79 & 80 WERE A.O.T. : RP4 PIN No's ADDED : E.L.

Title: SL502 MONO EQUALISER

Drg. No. T85002·73

Solid State Logic

SL 5000 M SERIES CONNECTOR CROSS REFERENCE

Introduction

Three main types of connector are used in SL 5000M series consoles.

Type	Identifier	Number of Pins
DIN 41612	DIN	32, 48, 64 or 96
Molex	MO	3, 5, 8 or 10
Ribbon (Scotchflex)	S	10, 16, 20, 26, 34, 40, 50 or 60
BICC	B	6, 10 or 19

= Harting
= Molex
= IDE
= PSU

As a general rule, the last two digits of a DIN connector number are the same as the last two digits of the cassette in which it appears; DIN connector numbers between DIN01 and DIN99 generally refer to the right-hand (logic) board of the cassette, numbers between DIN101 and DIN199 refer to the left-hand (audio) board. For example, DIN24 is the connector on the SL 524 Stereo Subgroup right-hand card. In the connector cross reference listings, all the DIN connectors for a particular cassette are grouped together.

For reasons of space, certain Instant Reset signals which appear on many of the DIN connectors are *not* fully cross-referenced. See the listings for S562 and S563 for details of these connections. Connections to three-pin Molex connectors are documented only in the listings of the relevant DIN connectors. Three-pin Molex connectors are usually used to handle a balanced signal, with the + and − components on pins 1 and 3, and 0V on pin 2.

In the listings of some DIN connectors, certain signals associated with addressing are given alternative cross references to ribbons. The actual cross reference will depend on the cassette's position within a block of (normally four) channels.

The 8-way Molex connector MO60 is used throughout the console. All non-standard connections to this connector are detailed in its listing.

B01 is a board-to-board connector which carries Total Recall/Instant Reset information where S562 and S563 cannot be fitted.

7 Connector Cross Reference

DIN02

From SL 502 Mono Eq
To EQ/Dynamics Bus

Page 1 of 2

Function	Pin No.	DIN02	MO80	MO81	MO98	MO102	S502	S532
Master Reset	1a							
Row Enable	2a							
IR A1	3a							
IR A3	4a							
IR A5	5a							
Spare (Bussed)	6a							10
Spare	7a							
Spare	8a							
Dyn. Link Send)	9a							4
Spare (Bussed)	10a							2
Key In +	11a		1					
0V	12a							
No connection	13a							
0V	14a							
+V Lamps	15a	15c						
+18V	16a	16c						
0V	17a	18a	2	2				
		17c						
0V	18a	17a						
		18c						
−18V	19a	19c						
−18V BU	20a	20c						
−25V	21a	21c						
−18V LEDS	22a	22c						
Spare to S502	23a						8	
Spare to S502	24a						9	
Spare to S502	25a						10	
Spare	26a							
Spare	27a							
Dyn. PRE Enable	28a						7	
EQ In	29a						5	
Return EQ/Dyn.	30a						2	
Interbus	31a						3	
Send EQ/Dyn.	32a						4	

DIN02

From SL 502 Mono Eq
To EQ/Dynamics Bus

Page 2 of 2

Function	Pin No.	DIN02	MO80	MO81	MO98	MO102	S502	S532
Analog Data	1c							
IR A0	2c							
IR A2	3c							
IR A4	4c							
Status Unlock	5c							
Spare (Bussed)	6c							9
Spare	7c							
Spare	8c							
Dyn. Link Send	9c							4
Spare (Bussed)	10c							1
Key In –	11c		3					
0V	12c							
No connection	13c							
0V	14c							
+V Lamps	15c	15a						
+18V	16c	16a						
0V	17c	17a				2		
		18c						
0V	18c	18a			2			
		17c						
–18V	19c	19a						
–18V BU	20c	20a						
–25V	21c	21a						
–18V LEDS	22c	22a						
Spare	23c							
Spare	24c							
Spare	25c							
Spare	26c							
Spare	27c							
Spare	28c							
Bal. Output –	29c					3		
Bal. Output +	30c					1		
Bal. Input –	31c				3			
Bal. Input +	32c				1			

MO60

POWER BUS

Function	Pin No.	DIN09	DIN103	DIN156	DIN257	DIN337	DIN357	Standard DINs	MO60
+V Lamps	1	2c		1b	1c			15a	
								15c	
+18V	2	1a	7a	1a		1a		16a	
			7b					16c	
			7c						
0V	3	1b	8a	1c	1b	2a		17a	4
			8b					17c	
			8c						
0V	4	1b	8a	1c	1b	3a		18a	3
			8b					18c	
			8c						
−18V	5	2a	9a	2a		4a		19a	
			9b					19c	
			9c						
−18V BU	6	2b	10a	2b		5a		20a	
			10b					20c	
			10c						
−25V	7	3a	11a	3a		6a	16b	21a	
		3b	11b	3b			16c	21c	
			11c						
−18V LEDS	8	1c	12a	2c		7a	15b	22a	
			12b				15c	22c	
			12c						

S502

From EQ/Dynamics Bus
To I/O Bus

Function	Pin No.	DIN01	DIN101	DIN105	DIN11	DIN111	DIN121
0V	1						
L.Return EQ/Dyn.	2		14c	14c		14a	14c
						14c	
L.Interbus	3						
L.Send EQ/Dyn.	4		14a	14a			14a
EQ In	5	32c			32c		
Spare	6						
Dyn. PRE Enable	7	30c			30c		
R.Return EQ/Dyn.	8						8c
R.Interbus	9						
R.Send EQ/Dyn.	10						8a

S532

Eq/Dynamics Channel Bus Links

Function	Pin No	DIN02	DIN10	DIN20	DIN22
Spare	1	10c	10c	10c	10c
Spare	2	10a	10a	10a	10a
Dyn. Link Send	4	9a	9a	9a	9a
		9c	9c	9c	9c
Spare	9	6c	6c	6c	6c
Spare	10	6a	6a	6a	6a

IR = Instant Recall = - Saving the status of all Switches
- Remoting all the switches by the SL581 Central Logic Unit

TR = Total Recall = Saving of all the Pots, for Rocking not really important

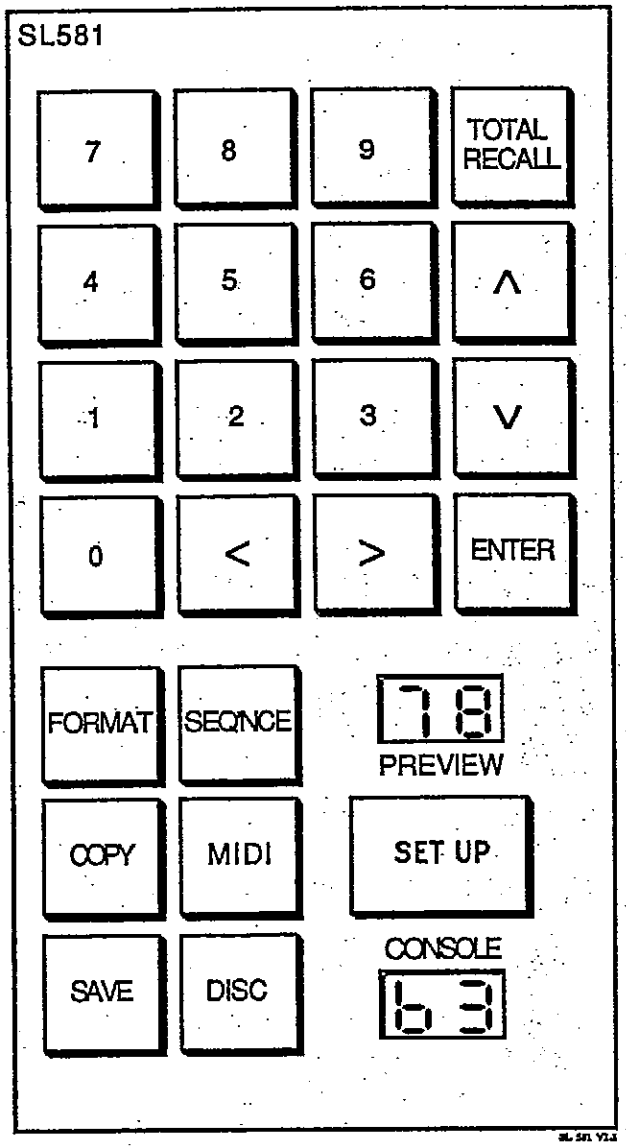


Figure 1. Front Panel Diagram

1. Introduction

The Instant Reset and Total Recall computer systems may be fitted to any SL 5000 M Series console. The Instant Reset Computer can instantly store and reset the states of the switches on virtually every cassette fitted in the console. The SL590 Total Recall facility allows the settings of rotary controls, faders, and switches on the console to be saved onto floppy disc by the operator.

Depending upon whether the Total Recall Computer is fitted, up to three modes of commands are available. These are known as Instant Reset Mode, Preview Mode, and Total Recall Mode respectively, and are described in Sections 2, 3, and 4 of this manual. Successive operation of the **TOTAL RECALL** key switches operation between the Instant Reset, Preview, and Total Recall Modes in turn.

The operator enters all commands via the keypad on the front panel of the SL581 Instant Reset Cassette. The front panel layout is shown in Figure 1 opposite.

Instant Reset Mode

The SL581 Instant Reset Computer allows a complete console 'Setup' to be restored with a simple keypad command. Up to eighty such Setups may be stored within the SL581. A further nine stores, known as *Formats*, are also available. Up to nine Sequences, each of a maximum of 99 stores in length, may also be memorised. A MIDI interface is incorporated which allows the SL581 to be controlled by external MIDI equipment.

The SL581 is supplied as a double-width cassette, the front panel of which contains a keypad and two displays. The keypad contains ten keys labelled **0 - 9**, which are used to identify the stored Setups. In addition, there are four Cursor keys, six Command keys labelled **FORMAT, SEQUENCE, COPY, MIDI, SAVE,** and **DISC,** two Utility keys labelled **TOTAL RECALL** and **SET UP,** and an **ENTER** key.

The two twin-character 7-segment displays are labelled **PREVIEW** and **CONSOLE.**

All of the Instant Reset Mode commands are described in Section 2 of this manual.

Preview Mode

The three additional commands available in Preview Mode allow the operator to quickly save and recall entire console Instant Reset and Total Recall Setups to and from disc, and to use the Total Recall monitor display to preview Setups stored on disc without affecting the state of the console.

The Preview Mode commands are described in Section 3 of this manual.

Total Recall Mode

The SL590 Total Recall Computer can quickly store the settings of all of the analogue controls on virtually every cassette described in this manual, regardless of the configuration and layout of the console. It is used in conjunction with the SL581 keypad and a colour graphics monitor.

The Total Recall facility allows the settings of rotary controls and faders on the SL 5000 M Series Console to be saved onto a floppy disc by the operator. When the operator wishes to recall these settings, a high-resolution image of the pot and fader settings is displayed on a

colour monitor, and any differences between the saved and current settings are highlighted. The operator can now adjust any console controls which do not match, and the monitor shows these changes as they occur. When the control is to within a predefined limit of the saved setting, the display highlight disappears to indicate a match.

5. Service Information

The information in this section is intended for the use of Service and Maintenance Personnel. The section begins with descriptions of how the console switches work and of how Instant Reset addresses the switches. Following a physical description of both the Instant Reset and Total Recall computers, circuit descriptions of the three user-serviceable cards are given. Finally, circuit test points for both systems are tabulated to aid fault diagnosis.

5.1 Instant Reset and the Console Switches

Switch circuitry on the SL 5000 M Series console differs radically from that of a standard on/off switch. Each switch on the console serves as an input to a digital circuit (one circuit for each switch), the output of which changes state each time that the switch is operated. Thus, if the output is 'low', it will be driven 'high' when the switch is operated, and vice versa. The output feeds to and controls console circuitry determined by the switch function. Also, the Instant Reset Computer monitors the state of this line for each console switch, and, when commanded, stores the current states ('high' or 'low') in memory.

Instant Reset can then use this stored data to reset the line at a later time. This is accomplished by means of a second input to the digital circuit (apart from the console switch). This input is driven from the Instant Reset Computer memory, and is capable of changing the state of the circuit output in the same way as the console switch. Figure 9 below shows the console switch operation a) by means of a simple block diagram and b) by means of an equivalent circuit.

A brief description of the equivalent circuit follows. Note that this circuit does not relate to the actual console switch design, and that it is included purely in order to assist the reader in understanding the concept.

Switch SW1 represents a typical console pushbutton switch. Each time that SW1 is pressed, flip-flop FF1 will toggle. Thus the state of the 'Q' output will change from 'high' to 'low', or vice versa, SO LONG AS THE 'MULTIPLEXER WRITE ENABLE' LINE IS 'LOW'. During this time the Instant Reset Computer may store the state of the 'Q' output of FF1 ('high' or 'low') in memory. This represents either an 'on' or 'off' state of the switch SW1.

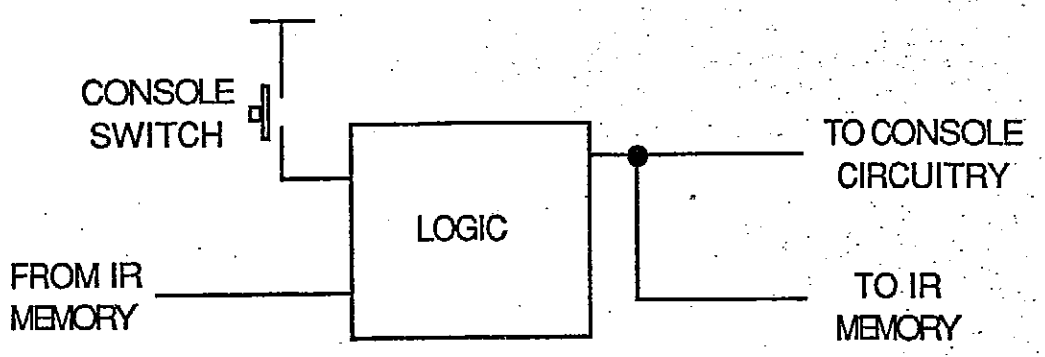


Figure 9a). Block Diagram of Console Switch operation

Now suppose that it is required to set SW1 back to this previously-stored state. This can be done by placing the stored state ('high' or 'low') from the Instant Reset memory on the 'SWITCH DATA' line, and by driving the 'MULTIPLEXER WRITE ENABLE' line 'high'. This will cause FF1 to be set 'high' or cleared 'low, independently of the state of SW1, due to

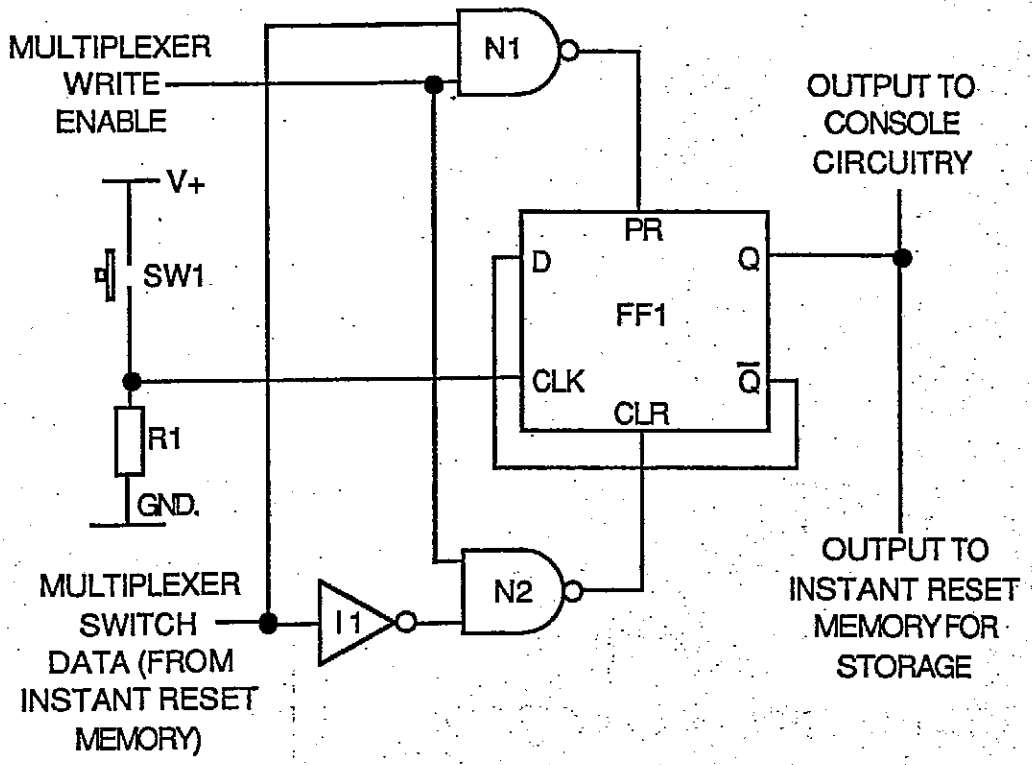


Figure 9b). Equivalent Circuit of Console Switch operation

the combination of NAND gates N1 and N2 and Inverter I1 driving the Preset (PR) and Clear (CLR) inputs of FF1.

Essentially, the two lines labelled 'Multiplexer Switch Data' and 'Output to Instant Reset memory' in Figure 9b) are the same line.

5.2 Instant Reset and Switch Addressing

It is now necessary to briefly describe how the SSL Address Bus architecture is able to address an individual cassette within up to 8 console channels, each with a maximum of 7 rows of cassettes.

It is convenient for the purposes of this discussion to consider eight console channels, each of them having seven rows of cassettes, and that none of the rows contains more than 1type of cassette.

The address signals available to each cassette comprise 6 Address Lines, and 7 Row Lines. In addition there are 8 Data Lines, each of which is connected to 1 of the 8 console channels. Consider now the case of changing the state of a single switch on a cassette.

Once the address signals for that switch (Row and Address Lines) have been set up by the computer and sent to the Multiplexer, not 1 but 8 switches will in fact now be addressed. These are a) the switch whose state is to be changed, and b) the equivalent switches on the other 7 console channels.

As the Row and Address Lines are set up, so are the Data Lines. Thus 1 Data Line represents the required 'new' state of 1 switch, and the other 7 Data Lines represent the existing states of the other 7 switches in the other channels. When all of this information is ready, it is output to the 8 cassettes. Thus, as it is only required to change the state of 1 switch, it is in fact necessary to output data representing the existing states of the other 7 (unchanged) switches to the equivalent 7 cassettes in the other 7 console channels.

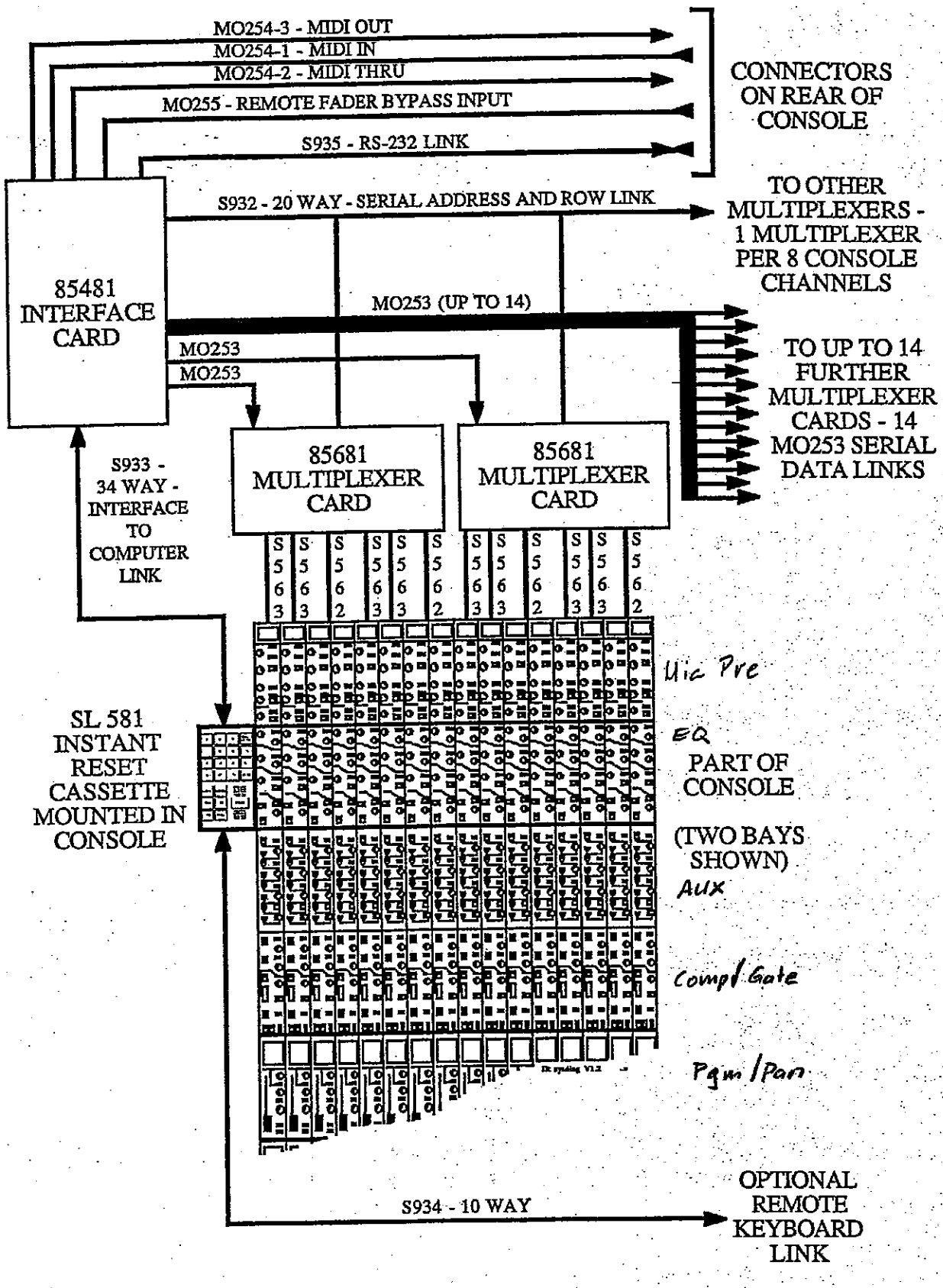


Figure 10. System Diagram of a typical Instant Reset installation

5.3 Physical Description

The SL581 is mostly contained within a double-width cassette, which contains a backplane assembly together with the following four circuit boards:

- The 85698 5k Mini Intelligent Peripheral Board (MIPI).
- The 85181 Battery Backup Board.
- The 85081 Switch Scanner Board.
- The 85281 Switch Support Board.

In addition the 85481 Interface Board and up to sixteen 85681Multiplexer Boards are mounted in the rear of the console. Figure 10 shows a System Diagram of a typical Instant Reset installation. Note that the Instant Reset computer communicates with the Total Recall computer (if fitted) via the MIDI interface.

5.3.1 85681 Multiplexer Board

Introduction

The 85681 Multiplexer Board handles 3 different data communications tasks. These are a) Writing switch data, b) Reading switch data, and c) Reading analog data. As the various data paths through the Multiplexer differ considerably for these 3 cases, each will be considered separately in the following sections.

Writing Switch Data

Address, Row, and Switch State Data are synchronously clocked into 3 Serial-to-Parallel shift registers, IC1, IC2, and IC3 respectively, by the ZCLK signal. Whilst the clocking of this data is taking place, the STROBE line is held HIGH, and the outputs of IC1-3 do not change state.

When the data clocking has been completed, the STROBE line is driven LOW, and the Address and Switch State data is directly latched to the outputs of IC1 and IC3. The Row data outputs from IC2 will only be enabled at this time if the Row Enable signal, RE, is present at IC26-A, and the Enable Sense line in the MO253 data cable from the Interface Board (See Section 4.1.5) turns off TR17, thus allowing IC26-A to enable IC2. If either of these conditions are not met, no data communication to or from the console channels can take place.

The 6 lines of address data from IC1 are buffered by IC4 to produce the 6 Address Lines, A0-A5, which are fed to the cassettes via connectors S563-1 to S563-4. The 7 lines of row data from IC2 are buffered in the same way by IC5 and IC6 to provide the 7 Row Lines, R1-R7, which are fed to the cassettes via connectors S562-1 and S562-2.

The /CA/BYPASS signal is fed via IC26-B and IC6-D to the S562 connectors. The STATUS UNLOCK signal, which originates in the SL557 Program Assign and Status Master Cassette, is buffered by IC26-C and IC6-E, the buffering being configured by link LK1. If the Multiplexer Board is connected to the console section containing the SL557, LK1 must be configured to INPUT. This allows the unbuffered STATUS UNLOCK signal received from the SL557 to be buffered to the remainder of the console. For Multiplexer Boards connected to all other console sections, LK1 should be configured to OUTPUT.

The 8 Data Lines, WD0-7, are fed from the outputs of IC3 to 8 discrete data buffers (IC8-18 and surrounding components). The writing of data through these buffers is controlled by the /RD/WR line being driven HIGH. The BIAS signal improves the switching characteristics of

the buffers. It prevents data corruption problems caused by slow switch-off times when driving capacitative loads such as the long lengths of ribbon cable used in the console. The buffered output lines, AD0-7, drive the 8 addressed cassettes with the required data.

Reading Switch Data

When reading switch data, Address and Row Data are clocked into IC1 and IC2 in exactly the same manner as when writing switch data (see section 4.1.6). When STROBE is driven low, the Address Lines A0-A5 and the Row Lines R1-R7 will be set up. The outputs of IC3 will also latch, but the discrete buffer stages (IC8-18 etc.) will adopt a high-impedance state as the /RD/WR line will be driven LOW.

Data representing the states of the 8 addressed switches will now appear on lines AD0-7, and hence on the Data Read Lines, RD0-7. These lines are fed to the parallel inputs of a shift register, IC19, that is clocked and synchronised by the ZCLK and STROBE signals respectively. When the STROBE next goes HIGH, the states of RD0-7 are 'jammed' into the 8 stages of this shift register. When ready to read the data the MIPI will drive the STROBE line LOW again, and issue 8 ZCLK pulses. Both the CS (ADC) and /RD/WR lines will be LOW, thus IC25-B will be enabled, and the data will be clocked out of the 'Q8' pin of IC19, through IC25-B, and thence back to the MIPI via the balanced DATA lines. Note that during the data clocking period, even though the data transitions will pass to the DATA WR line via IC24-B, the data will NOT be clocked back into the Data Write Shift Register, IC3, because the STROBE line is LOW.

Reading Analog Data

The multiplexer reads analog data, typically from faders and potentiometers, by addressing these devices in the same way as for switches. It feeds the analog signals so obtained through an analog-to-digital converter (ADC) which converts the signals to digital data streams for transmission to the MIPI.

When reading analog data, Address and Row Data are clocked into IC1and IC2 in exactly the same manner as when writing switch data (see section 4.1.6). When STROBE is driven low, the Address Lines A0-A5 and the Row Lines R1-R7 will be set up. The outputs of IC3 will also latch, but the discrete buffer stages (IC8-18 etc.) will adopt a high-impedance state as the /RD/WR line will be driven LOW.

Analog voltages from the addressed faders or potentiometers will now appear on lines AD0-7, and hence on the Data Read lines, RD0-7. These lines are fed via analog switches IC20 and IC21 to the multiplexed inputs of an ADC, IC7. A precision voltage reference for the ADC is supplied by D32. Inverters IC17-E and -F and R4, R5, and C2 form the ADC system clock, which runs at around 2 MHz.. Input and output of serial data to and from the ADC is clocked by ZCLK. ADC Multiplexer channel address data appears on the MUX line. The operational ADC cycle will now be described.

When the MIPI drives the CS (ADC) line HIGH, the analog switches are closed, the ADC output is enabled via IC18-E, and IC25-A is enabled. The ADC now waits for 2 RISING edges and 1 FALLING edge of the system clock, after which it places the MSB of the previous conversion result on the DOUT pin.

The next 4-bit multiplexer channel address is shifted in on the first 4 RISING edges of ZCLK, the MSB of the address being shifted in first. The FALLING edges of these same 4 ZCLK pulses shift out the second, third, fourth, and fifth MS bits of the previous conversion result.

The ADC now begins to sample the analog voltage specified by the new address data. Another 3 ZCLK pulses complete the shifting out of the previous conversion data, which feeds via IC25-A to the MIPI via the balanced DATA lines.

The FALLING edge of the next ZCLK pulse completes the analog sampling process and starts the hold and conversion function. Conversion is performed during the next 36 ADC system clock cycles. The CS (ADC) now returns LOW to allow until after the conversion is complete.

When the CS (ADC) line is next driven HIGH, the process repeats,with the serial data representing the last selected multiplexer channel address appearing at the ADC output as the latest cycle progresses as described above.

5.3.2 85481 Interface Board

The bus control signals, CS (ADC), STROBE, ADDR, MUX, BIAS, ROW, ROWEN, and /RD/WR, are buffered by IC1 before being fed to Balanced Line Drivers, IC2-3. The balanced output signals from these devices feed directly to the Multiplexer Board(s). The STATUS UNLOCK signal is tied to Vcc by R3, but is not otherwise processed.The clock input ZCLK is fed into a monostable, IC5-A, which stretches the signal pulse width to around 2 uSec. This modified clock signal is then fed to a Balanced Line Driver, IC4-A, and thence to the Multiplexer Board(s).

There are 16 bidirectional serial data lines on the bus. These are driven by PIO 1 on the MIPI, and 1 data line per Multiplexer is required. The 16 lines enter the Interface Board via 2 8-bit Bus Transceivers, IC6 and IC12. Each line from the 'inboard' side of these devices then connects to a pair of chips, IC8-9, IC10-11, IC13-14, and IC15-16, configured as a Balanced Line Driver and Receiver stage. The 'outboard' side of each chip pair connects to a Multiplexer Board as a bi-directional balanced line via 1 of 16 MO253 connectors.Pin 2 of each MO253 connector is the Multiplexer Enable Sense line, and is connected to Vss. Data direction control through the Interface Board is controlled by the /RD/WR line from IC6 and the inverse of this signal generated by IC7-A.

The Diagnostic Interface RS232 buffers, IC22-23, are level shifted by Optocouplers IC18-21 and give RS232 levels for the outputs and TTL logic levels for the inputs.

The MIDI input is opto-isolated and buffered by IC24, the output of which feeds to the MIDI IN line on the MIPI and, via inverters IC7-E and -F, to the MIDI THRU connector.

The Remote Bypass Input is rectified by WO1, and opto-isolated and buffered by IC17. The output of IC17 feeds 2 inverters, IC7-B and -C, connected in series. Link LK1 allows for selection of the polarity of the /CA/BYPASS output signal to the Multiplexers, or for this signal to be permanently tied high or low.

Regulated voltages to drive the various interfacing circuitry on this board are provided by IC49 (+ 12v.), IC50 (+ 5v.), and IC51 (- 12v.).

5.4 Instant Reset Computer Faultfinding

5.4.1 MIPI Test Points and Links

- TP1- Clock (4MHz.).
- TP2- SCLK (4MHz.).
- TP3- /M1 (CPU chip).
- TP4- FCLK (4MHz.).
- TP5- /O7 of Address Decoder.
- TP6- /O6 of Address Decoder.

The 2 RAM chips may be of up to 16 k Bytes by 8 bits each. Their chip select inputs (/CS) are driven by /RAM0 and /RAM1 respectively. Both Write Enable lines (/WE) are driven by the /WR signal, and both Output Enable lines (/OE) are driven by the /RD signal. Either 24- or 28-pin RAM chips may be fitted, and links LK3 (for IC1) and LK2 (for IC7) allow the configuration of pin 26 of the 28-pin socket to either Vcc (for 24-pin devices) or Address Line A13 (for 28-pin devices). For situations where a 24-pin device is used for IC7, an additional link, LK1, is provided to configure pin 23 of the 28-pin socket (i.e. pin 21 of a 24-pin device) to either the /WR signal or to Address Line A11.

5.4.2 Battery Backup Board Test Points and Links

There are no test points or links on the Battery Backup Board.

5.4.3 Switch Scanner Board Test Points and Links

- TP1- Vss (-25 v.).
- TP2- SD CLOCK.
- TP3- SD LEDS.
- TP4- SD LAMPS.
- TP5- SW DATA.
- TP6- SW CLK.
- TP7- SW STROBE.
- TP8- Test output - IC6 Pin 9.

The switch scanner is a 24-stage parallel-to-serial shift register,comprising IC3, IC4, and IC4. The switch states appear at the parallel inputs, P1 - P8, of these devices. As there are only 23 switches, the remaining input, P1 of IC5, is held low via RP7 or may be tied high via link LK1. Whilst the SW STROBE line is held low, no parallel-to-serial conversion takes place, and the shift register remains entirely transparent to changing switch states. When this line switches high, P1 - P8 are disabled, and serial data representing the switch states is clocked out to the SW DATA line by the SW CLK signal.

The switches are scanned at approximately 8 mSec. intervals.

NOTE THAT LINK LK1 MUST BE FITTED IN THE 'SPARE' POSITION, AND NOT TO Vcc.

5.4.4 Interface Board Test Points and Links

- TP1- Vss.
- TP2- CA/BYPASS.

Link LK1 allows for selection of the polarity of the /CA/BYPASS output signal to the Multiplexers, or for this signal to be permanently tied high or low.

5.4.5 Multiplexer Board Test Points and Links

- TP1- Vss.
- TP2- RE.
- TP3- STROBE.
- TP4- SCLK.

The /CA/BYPASS Signal is fed via IC26-B and IC6-D to the S562 connectors. The STATUS UNLOCK signal, which originates in the SL557 Program Assign and Status Master Cassette, is buffered by IC26-C and IC6-E, the buffering being configured by link LK1. If the Multiplexer Board is connected to the console section containing the SL557, LK1 must be configured to INPUT. This allows the unbuffered STATUS UNLOCK signal received from the SL557 to be buffered to the remainder of the console. For Multiplexer Boards connected to all other console sections, LK1 should be configured to OUTPUT.

5.5 Total Recall Computer Faultfinding

5.5.1 Servicing Information

The SL590 Total Recall circuitry is made up of four proprietary cards and one SSL-manufactured card, the RS-232 to MIDI Interface Card. The proprietary cards are not user-serviceable, and any faults found in these cards as a result of running the diagnostic routines will require that the appropriate card be replaced. A brief circuit description of the RS-232 to MIDI Interface Card is given below for the benefit of service personnel.

5.5.1.1 The RS-232 to MIDI Interface Card

This card provides a bi-directional interface between RS-232 and MIDI signal levels. Transmitted Data at pin 1 of SO1 feeds a Line Receiver, IC1-A, the output of which is buffered by IC3-A before feeding to the MIDI connector MO254-3. Received Data from connector MO254-1 is opto-isolated and buffered by IC24, the output of which is interfaced to the RXD line on socket SO1 by Line Driver IC2-A and to the MO254-2connector by IC3-B. LED D2 provides indication of +5 V. supply availability on the card. Test points TP1-3 may be used to check the levels of the +12 V., -12 V., and +5 V. supplies respectively.

5.5.2 Configuration Information

The links on the proprietary cards, the power supply, and the disc drives must be configured correctly before they are installed in the SL590. The link locations are described for cards lying component side uppermost with the DIN connector on the left. *Note that configuration data for two types of Processor and Floppy Disc Cards are given: either type may be fitted.*

6 Connector Details

6.1 Connector Pin-Outs

Connector Name : **S562** - There are two per console bay, designated **S562-1** and **S562-2**
Location : Link between MUX Card and Console Backplane
Connector Type : 10 - way ribbon connector
Connector Function : Carries Row data to cassettes (R1-7)

Pin Number	Function
1	R1
2	R2
3	R3
4	R4
5	R5
6	R6
7	R7
8	CA/BYPASS
9	Status Unlock

Connector Name : **S563** - There are four per console bay, designated **S563-1** to **S563-4**
Location : Link between MUX Card and Console Backplane
Connector Type : 10 - way ribbon connector
Connector Function : Carries Address data to cassettes

Pin Number	Function
1	Status Unlock
2	SEE TABLE BELOW
3	Master Reset
4	A0
5	A1
6	A2
7	A3
8	A4
9	A5
10	SEE TABLE BELOW

The functions of pins 2 and 10 differ according to the following table:

Connector	Pin 2 Function	Pin 10 Function
S563-1	AD1	AD0
S563-2	AD3	AD2
S563-3	AD5	AD4
S563-4	AD7	AD6

Connector Name	:	S932
Location	:	Daisychain link between Interface Card and up to sixteen Multiplexer Cards on rear of console
Connector Type	:	20 - way ribbon connector
Connector Function	:	Carries balanced Cassette Address and Row Data signals from Interface Card to Multiplexer Cards

Pin Number	Function
1	CS (ADC)+
2	CS (ADC)-
3	SCLK+
4	SCLK-
5	STROBE+
6	STROBE-
7	ADDR+
8	ADDR-
9	RD/WR+
10	RD/WR-
11	MUX+
12	MUX-
13	BIAS+
14	BIAS-
15	ROW+
16	ROW-
17	ROW EN+
18	ROW EN-
19	STATUS UNLOCK
20	CA/BYPASS

Connector Name : S933
Location : Link between SL581 Instant Reset Cassette and Interface Card on rear of console

Connector Type : 34 - way ribbon connector
Connector Function : Carries Cassette Address, Row, and Switch Data signals from Instant Reset Computer to Interface Card

Pin Number	Function
1	DX0: Multiplexer 1 Switch Data
2	DX1: Multiplexer 2 Switch Data
3	DX2: Multiplexer 3 Switch Data
4	DX3: Multiplexer 4 Switch Data
5	DX4: Multiplexer 5 Switch Data
6	DX5: Multiplexer 6 Switch Data
7	DX6: Multiplexer 7 Switch Data
8	DX7: Multiplexer 8 Switch Data
9	DX8: Multiplexer 9 Switch Data
10	DX9: Multiplexer 10 Switch Data
11	DX10: Multiplexer 11 Switch Data
12	DX11: Multiplexer 12 Switch Data
13	DX12: Multiplexer 13 Switch Data
14	DX13: Multiplexer 14 Switch Data
15	DX14: Multiplexer 15 Switch Data
16	DX15: Multiplexer 16 Switch Data
17	-25 V.
18	SCLK
19	CS ADC
20	STROBE
21	ADDR
22	RD/WR
23	MUX
24	BIAS
25	ROW
26	ROW EN
27	STATUS UNLOCK (from S932 pin 19)
28	MIDI IN
29	RX Data (from RS-232 I/F)
30	MIDI OUT
31	TX Data (to RS-232 I/F)
32	CTS (to RS-232 I/F)
33	RTS (from RS-232 I/F)
34	-25 V.

Connector Name : S934
Location : Link between SL581 Instant Reset Cassette Bus Cards to permit remote keypad operation
Connector Type : 10 - way ribbon connector
Connector Function : Carries all signals which control front panel lamp and switch functions. Keypads of cassettes linked by this connector will operate in parallel.

Pin Number	Function
1	SD LAMPS
2	SD LEDS
3	SD CLK
4	
5	
6	
7	
8	SW DATA
9	SW CLK
10	SW STROBE

Connector Name : S935
Location : RS-232 link between Interface Card and 25-way 'D' type connector on Console Connector Panel
Connector Type : 26 - way ribbon connector (line 26 not used)
Connector Function : Carries RS-232 signals used when in Diagnostic mode to communicate with a terminal

Pin Number	Function
1	Ground
3	Transmitted Data (TxD)
5	Received Data (RxD)
7	Request To Send (RTS)
9	Clear To Send (CTS)
13	Ground
All other pins	Unused

Connector Name : MO253
Location : Link between Interface Card and Multiplexer Card (Up to sixteen MO253 connectors per Interface Card)
Connector Type : 3 - way polarised Molex connector
Connector Function : Carries Multiplexer Switch data from Interface Card to Multiplexer Card

Pin Number	Function
1	Data +ve
2	Enable Sense (-25 v)
3	Data -ve

Connector Name	:	MO254-1, MO254-2, MO254-3
Location	:	Links from Interface Card to Console Connector Panel
Connector Type	:	3 - way polarised Molex connector
Connector Function	:	Carries MIDI data between Interface Card and external devices: MO254-1 is MIDI IN, MO254-2 is MIDI THRU, MO254-3 is MIDI OUT

Pin Number	Function
1	MIDI +ve
2	Shield
3	MIDI -ve

Connector Name	:	MO255
Location	:	Links from Interface Card to Console Connector Panel
Connector Type	:	3 - way polarised Molex connector
Connector Function	:	Remote Bypass Input Connector

Pin Number	Function
1	Remote Bypass +/-
2	n/c
3	Remote Bypass -/+

(Note that signals of *either* polarity are acceptable)

6.2 Connector Cross Reference Tables

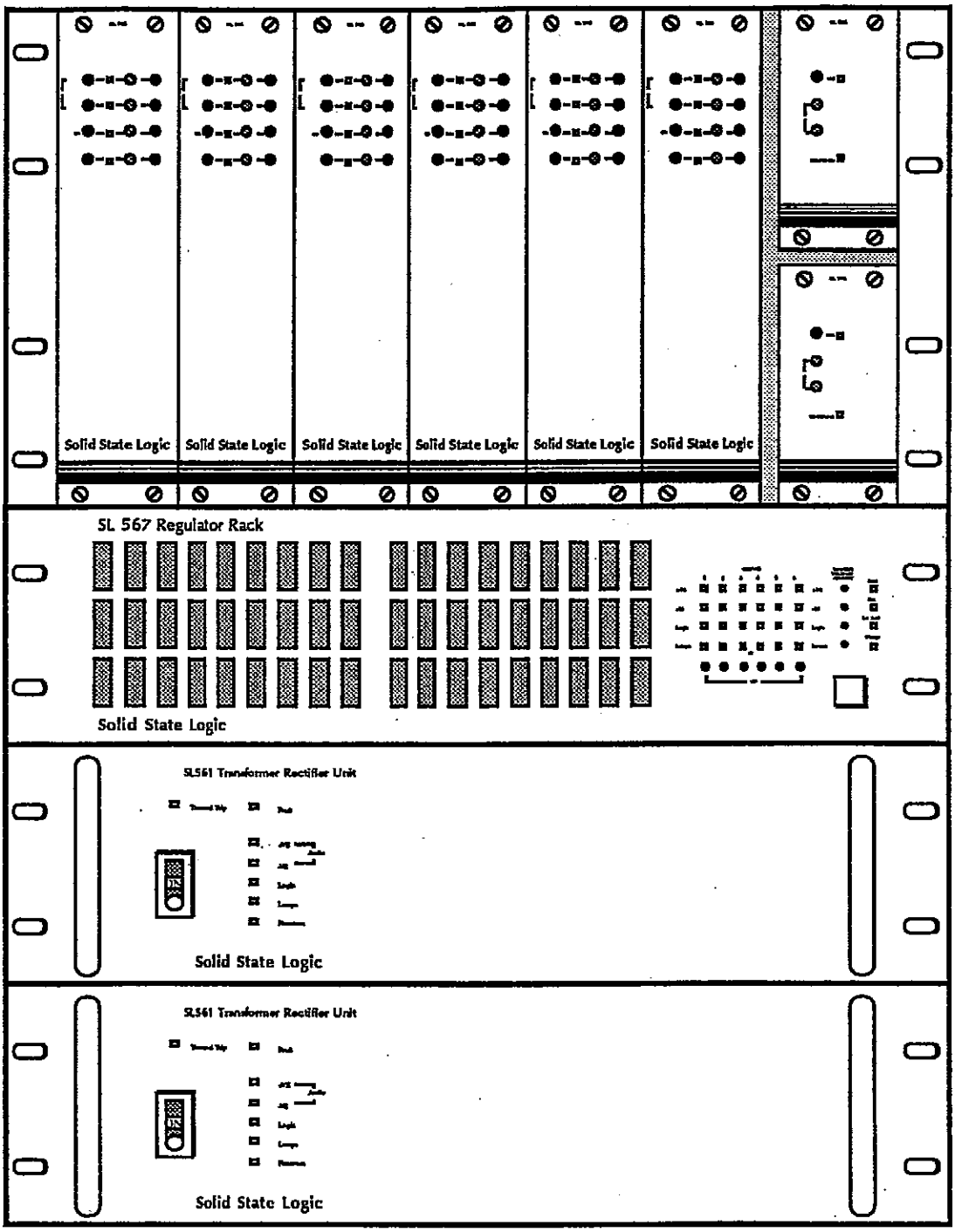
Function/Name	DIN128	S933	S932	MO60	DIN81	S934-1
GND. (-25 v.)	1a	17, 34		7	21a, b, c	
GND. (-25 v.)	1b	17, 34		7	21a, b, c	
GND. (-25 v.)	1c	17, 34		7	21a, b, c	
MI2+	2a			8	22a, b, c	
TR0 (IC 2 Pin 23)	2b					
MI1+	2c			8	22a, b, c	
MI2-	3a	29				
ZC0 (IC 2 Pin 7)	3b					
MI1-	3c	28				
MO2+	4a					
TR1 (IC 2 Pin 22)	4b					
MO1+	4c					
MO2- RS-232 Out	5a	31				
ZC1 (IC 2 Pin 8)	5b					
MO1- MIDI Out	5c	30				
GND. (-25 v.)	6a					
GND. (-25 v.)	6b					
GND. (-25 v.)	6c					
n/c (RXD)	7a					
TR2 (IC 2 Pin 21)	7b					
n/c (TXD)	7c					
RTS	8a	32				
ZC2 (IC 2 Pin 9)	8b					
CTS	8c	33				
GND. (-25 v.)	9a					
GND. (-25 v.)	9b					
GND. (-25 v.)	9c					
SCLK	10a	18				
TR3 (IC 2 Pin 20)	10b					
BSTB (IC 16 Pin 17)	10c			7		
DX 9 (IC 16 Pin 28)	11a	10				
2 MHz. (IC 9 Pin 4)	11b					
DX 8 (IC 16 Pin 27)	11c	9				
DX 11 (IC 16 Pin 30)	12a	12				
1 MHz. (IC 9 Pin 5)	12b					
DX 10 (IC 16 Pin 29)	12c	11				
DX 13 (IC 16 Pin 32)	13a	14				
C1 (IC 9 Pin 13)	13b					
DX 12 (IC 16 Pin 31)	13c	13				
DX 15 (IC 16 Pin 34)	14a	16				
QA (IC 9 Pin 11)	14b					
DX 14 (IC 16 Pin 33)	14c	15				
n/c	15a					
QB (IC 9 Pin 10)	15b					
ASTB (IC 16 Pin 16)	15c					
DX 1 (IC 16 Pin 14)	16a	2				
QC (IC 9 Pin 9)	16b					

Function/Name	DIN128	S933	S932	MO60	DIN81	S934-1
DX 0 (IC 16 Pin 15)	16c	1				
DX 3 (IC 16 Pin 12)	17a	4				
QD (IC 9 Pin 8)	17b					
DX 2 (IC 16 Pin 13)	17c	3				
DX 5 (IC 16 Pin 9)	18a	6				
ACLK	18b					
DX 4 (IC 16 Pin 10)	18c	5				
DX 7 (IC 16 Pin 7)	19a	8				
n/c	19b					
DX 6 (IC 16 Pin 8)	19c	7				
GND. (-25 v.)	20a					
n/c	20b					
GND. (-25 v.)	20c					
BRDY (IC20 Pin 21)	21a					
n/c	21b					
BSTB (IC20 Pin 17)	21c					
Sd Lamps (IC20 Pin 28)	22a				10c	1
n/c	22b					
Sd Clk (IC20 Pin 27)	22c				10a	3
St. Unlock (IC20 Pin 30)	23a	27	19			
n/c	23b					
Sd LEDs (IC20 Pin 29)	23c				9a	2
Sw Strobe (IC20 Pin 32)	24a				8c	10
n/c	24b					
Sw Clk (IC20 Pin 31)	24c				8a	9
(IC20 Pin 34)	25a					
n/c	25b					
(IC20 Pin 33)	25c				7a	8
ARDY (IC20 Pin 18)	26a					
n/c	26b					
ASTB (IC20 Pin 16)	26c					
CS (ADC) (IC20 Pin 14)	27a					
n/c	27b					
BIAS (IC20 Pin 15)	27c	24				
ROW EN (IC20 Pin 12)	28a	26				
n/c	28b					
RD/WR (IC20 Pin 13)	28c	22				
ADDR (IC20 Pin 9)	29a	21				
n/c	29b					
ROW (IC20 Pin 10)	29c	25				
MUX (IC20 Pin 7)	30a	23				
n/c	30b					
STROBE (IC20 Pin 8)	30c	20				
n/c	31a					
n/c	31b					
n/c	31c					
Vcc (-18 v.)	32a					
Vcc (-18 v.)	32b					
Vcc (-18 v.)	32c					

Function/Name	DIN81	MO60	S934-1	S934-2
	1a			
	1b			
	1c			
	2a			
	2b			
	2c			
	3a			
	3b			
	3c			
	4a			
	4b			
	4c			
	5a			
	5b			
	5c			
	6a			
	6b			
	6c			
Sw Data In	7a		8	
	7b			
	7c			
Sw Clk In	8a		9	
	8b			
Sw Strobe In	8c		10	
Sw LEDs In	9a		2	
	9b			
	9c			
Sd Clk In	10a		3	
	10b			
Sd Lamps In	10c		1	
	11a			
	11b			
	11c			
	12a			
	12b			
	12c			
	13a			
	13b			
	13c			
	14a			
	14b			
	14c			
Lamps	15a	1		
Lamps	15b	1		
Lamps	15c	1		
	16a			
	16b			
	16c			
0 V	17a	3,4		
0 V	17b	3,4		
0 V	17c	3,4		

Function/Name	DIN81	MO60	S934-1	S934-2
0 V	18a	3,4		
0 V	18b	3,4		
0 V	18c	3,4		
	19a			
	19b			
	19c			
	20a			
	20b			
	20c			
-25 V	21a	7		
-25 V	21b	7		
-25 V	21c	7		
LEDs	22a	8		
LEDs	22b	8		
LEDs	22c	8		
	23a			
	23b			
	23c			
	24a			
	24b			
	24c			
	25a			
	25b			
	25c			
	26a			
	26b			
	26c			
	27a			
	27b			
	27c			
	28a			
	28b			
	28c			
Sw Data Out	29a			8
	29b			
	29c			
Sw Clk Out	30a			9
	30b			
Sw Strobe Out	30c			10
Sd LEDs Out	31a			2
	31b			
	31c			
Sd Clk Out	32a			3
	32b			
Sd Lamps Out	32c			1

SL561: SL 5000 M Series Power Supply System



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1. Introduction

The SL5000 M Series Power Supply System comprises the following modules:

The SL561 Transformer and Rectifier Unit
The SL565 Voltage Regulator Card
The SL566 Phantom Power Regulator Card
The SL567 Regulator Rack

These system components may be configured in a great variety of ways to suit the power requirements of any possible console configuration. The design allows the principal components to be bussed together in situations where either extra power is required or backup in the event of failure is deemed essential. A system diagram of a typical SL 5000 M console power supply is shown in Figure 3 at the end of this section.

Circuit descriptions are provided as appropriate, together with all information required for the correct set-up, configuration, and adjustment of each module. A brief functional description of each of the modules follows.

1.2 The SL561 Transformer and Rectifier Unit

The SL561 Transformer and Rectifier Unit converts the a.c. Mains input into unregulated d.c. output voltages. The outputs from the SL561 connect to the input side of the SL567 backplane bus (see below), and feed via the backplane to the inputs of the SL565 and SL566 regulator cards. *No more than 1500VA must be drawn from the unit.* The outputs are diode-isolated and more than one SL561 may therefore be connected in parallel, thus providing a means of ensuring that supply to the console is maintained in the event of failure of one of the units. The SL561 is shown in Figure 1. It is supplied as a 3U-high 19" rack-mounting package, of depth 360 mm.

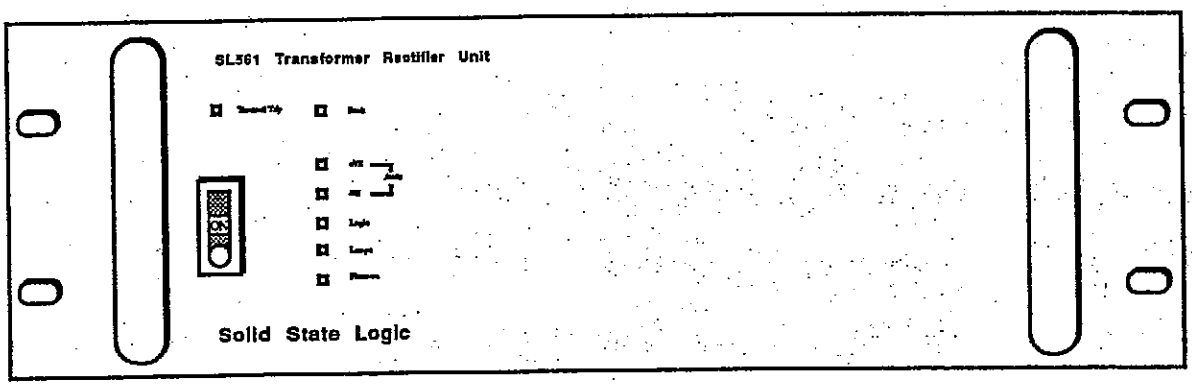


Figure 1. The SL561 Transformer Rectifier Unit Front Panel.

1.1 The SL567 Regulator Rack

The SL567 Regulator Rack comprises the Backplane Assembly into which the SL565 and SL566 Regulator modules connect, and the Power Rail Monitoring circuitry. The output voltages from the regulator modules feed from this backplane bus via the monitoring circuitry to the console. The SL567 can accommodate up to six SL565 and two SL566 modules. It is supplied as a 9U-high 19" rack-mounting package, of depth 360 mm. The SL567 incorporates an Alarm Sounder bus and a Power Fail Relay bus, both of which may be used to signal the failure of any of the regulators fitted in the SL567 Rack.

The Power Rail Monitor is located directly below the Regulator Rack. The main functions of this unit are to monitor the current drawn by the console, to isolate the console from the power supply if a fault is detected, and to provide a Battery Backup Supply to the console in the event of a power failure.

Master voltage adjustment potentiometers for the SL565 modules are provided on the front panel of the Power Rail Monitor.

1.3 The SL565 Voltage Regulator Card

The SL565 Voltage Regulator Card converts the raw d.c. voltages generated by the SL561 into regulated d.c. voltages. Each SL565 card provides five regulated outputs at +18V, -18V (two outputs), +5V, and -24V. Each of these outputs can supply a maximum current of 4 Amps, or up to 5 Amps when the card is fan-cooled. A further 15V regulated output (relative to the -24V line) is provided to power up to two console fans.

The + and - 18V outputs provide a balanced supply for the audio circuitry. The -24V output constitutes the negative line for both the lamp and logic supplies. These comprise the +5V and the second -18V output respectively, the arrangement thus providing 29 volts for the lamp supply and 6 volts for the logic supply, both relative to the -24V line. All outputs are provided with thyristor 'crowbar' protection against excessive voltage transients which might damage console circuitry. The + and - 18V audio supplies are equipped with further protection circuitry which causes either output to shut down if the other is not present. A pair of normally open relay contacts, which close if a fault is detected within the module, is incorporated, together with an output to the SL567 Alarm Sounder Bus (see Section 1.1).

Adjustment potentiometers for the +18V, +5V, and the two -18V outputs are accessible from the front panel. Test sockets are provided on the front panel for use when checking or adjusting the voltage levels. Front panel LED indicators are provided for the AUDIO +VE, AUDIO -VE, LOGIC, and LAMPS voltage outputs.

The SL565 is designed to operate in parallel with other SL565 cards in applications where the maximum current output limit for one card (see above) would be exceeded. For such applications, circuitry is provided to allow each of the the four outputs to be remotely adjusted by a master control. *Note that the master control can only adjust the regulator outputs upwards from their individually set voltage levels.*

1.4 The SL566 Phantom Power Regulator Card

The SL566 Phantom Power Regulator Card generates a regulated +48V d.c. supply required by capacitor microphones. The type of circuitry is broadly similar to that of the SL565 module described above. The SL566 is designed to operate in parallel with other SL566 modules in applications where the power consumption exceeds the 0.5 Amps maximum limit. In addition, a pair of normally open relay contacts, which close if a fault is detected within the module, is incorporated. This may be used to switch an external alarm in the event of failure. An integral warning buzzer connects via the backplane connector to the Alarm Sounder Bus of the SL567, and may thus be activated if either the SL566 or any of the SL565 Regulator Cards fail.

An output adjustment potentiometer is accessible from the front panel. Test sockets are provided on the front panel for use when checking or adjusting the voltage level.

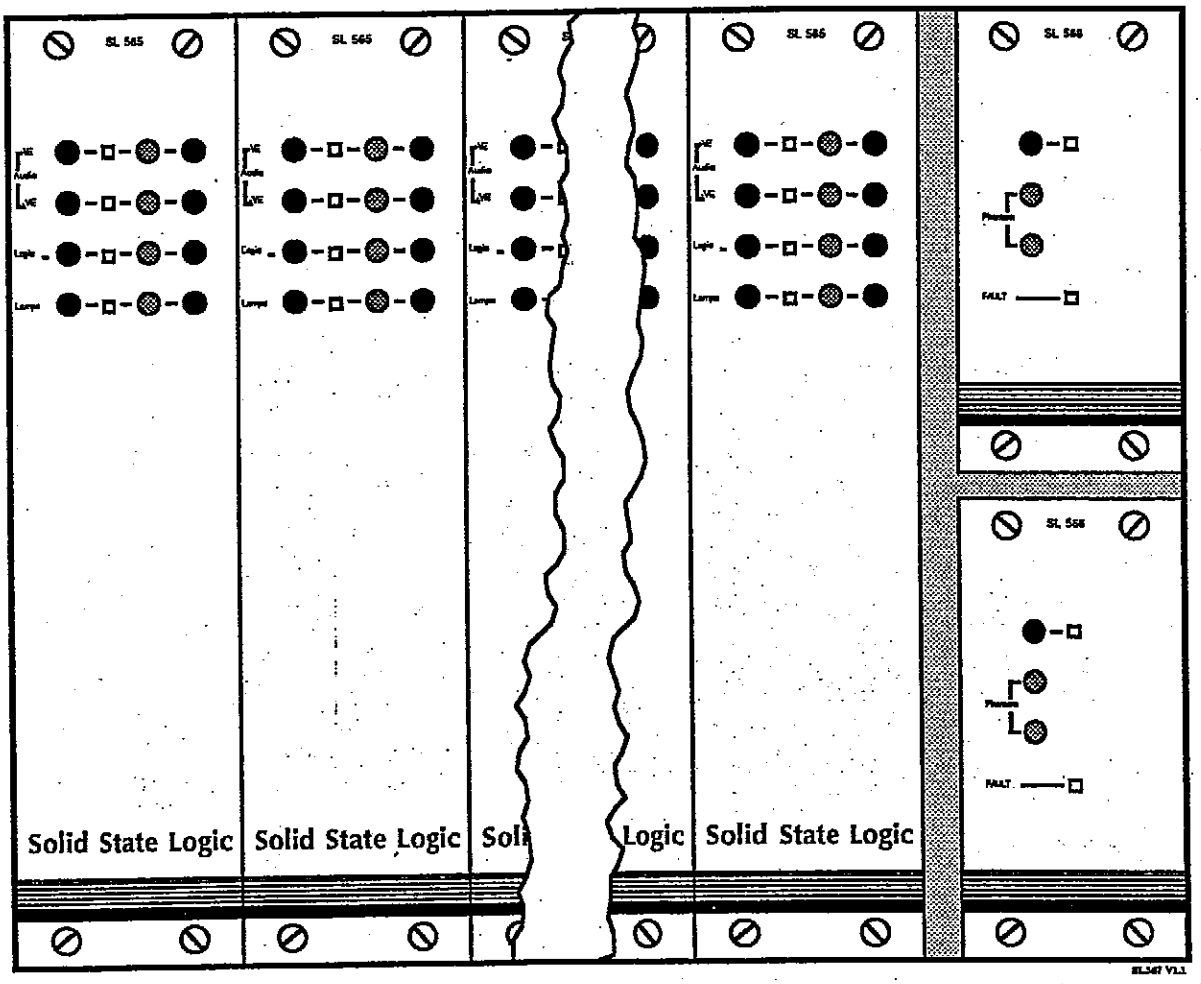


Figure 2. Arrangement of SL565 and SL566 Regulators within the SL567 rack

1.6 The Power Distribution/Fan Driver Monitor Cards

These cards are located throughout the console, a minimum of one card per console bay being required. Each card receives power from the rack assembly via 19-way BICC connectors on the console back panel, and distributes it to the cassette bus cards via MO60 connectors. Each card also provides drive and failure monitoring circuitry for up to two fans.

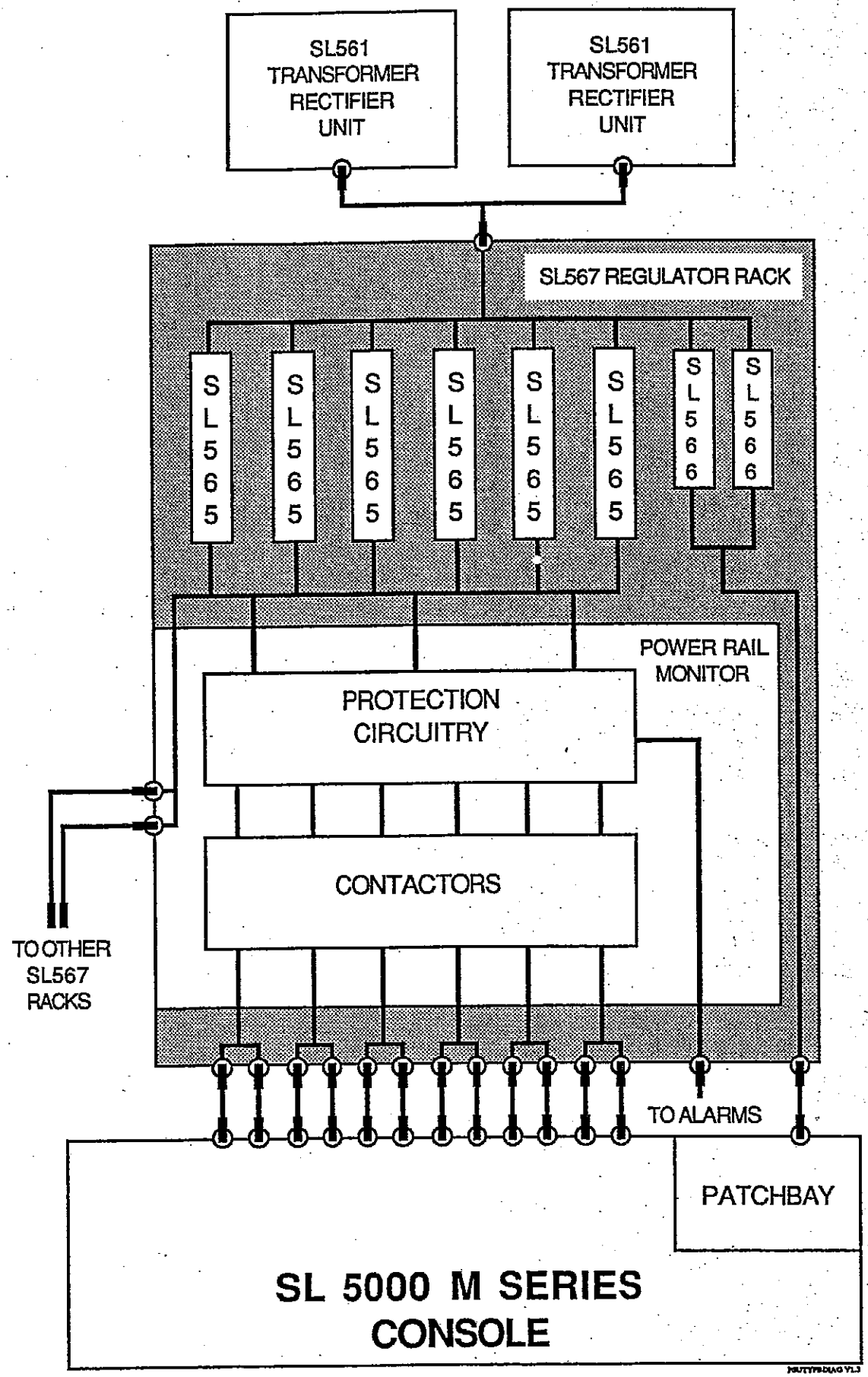


Figure 3. A typical Power Supply System Diagram

2. Circuit Descriptions

The circuits of each of the constituent modules of the SL561 Power Supply System are described in the following sections. Component references are made with respect to the appropriate drawings.

2.1 The SL561 Transformer and Rectifier Unit (Drawings T85161.71, T85261.71)

The mains input feeds via the mains switch and a fuse, FS1, to a transformer, TX2. The 24V a.c. secondary of TX2 drives a contactor via the mains transformer thermal trip, THT1, and the rectifier heatsink thermal trip, THT2.

The secondary also feeds bridge rectifier BR1, which, together with regulator REG1 and associated components, provides power for the fan, FAN1.

A red LED is driven from the a.c. input to BR1 via R4 and the contactor to provide 'THERMAL TRIP' indication whenever thermal switches THT1 or THT2 break and allow the contactor to drop out.

Note that BR1, REG1, R4 and associated components are all fitted on the 85261 Low Voltage Regulator board.

When the contactor is energised, mains is supplied via two pairs of contacts to transformer TX1. The transformer has five secondaries, two each at 23.5V and one each at 52V, 32.5V, and 12V, and can supply a maximum of 1500VA *shared between these five outputs*. Each of these secondaries drives an associated bridge rectifier, BR1-5. The rectified voltages from BR1-5 are smoothed by capacitors C1-7 before being fed via series diodes to the 85161 Unregulated d.c. Distribution Card. From here they are sent to the SL565 and SL566 regulator modules and power fail sense circuitry.

Each of the five rectified voltages drive an opto-isolator, OPT1-5, and LED, LED1-5, via associated resistors. The LEDs provide 'power available' indication for each of the voltages.

OPT1-5 together with comparator IC6 and associated circuitry provide power failure sensing. The outputs of the opto-isolators are connected in series with resistor R22 across the power rails of IC6, and connect to the non-inverting input of IC6 via R23. (This forms the logical equivalent of a 5-input NAND gate connected to IC6, the inputs to the NAND gate being the 5 rectified supplies.) The inverting input of IC6 is set nominally at 0.6 of the supply voltage by R24-25, and D5-6 constrain the non-inverting input of IC6 to within ±0.7V of the inverting input. Should any of the rectified voltages fail, the relevant opto-isolator OPT1-5 will switch off. This will cause R22-23 to pull the non-inverting input of IC6 high, thus driving the output of IC6 high. The 'FAULT' LED, LED6, will now light, relay RL1 will be energised, and the piezo sounder SD1 will provide an audible warning if the associated link is fitted. (RL1, LED6, and SD1 are all driven from the output of IC6.) The 'power available' LED associated with the failed voltage will also extinguish.

2.2 The SL565 Voltage Regulator Card (Drawings T85065.71-3)

The SL565 contains four regulator circuits which provide the AUDIO +VE, AUDIO -VE, LAMPS +VE, and LOGIC +VE outputs, and a fifth regulator which provides power for up to two console fans. The two AUDIO outputs are generated relative to the AUDIO 0V line, and the LAMPS +VE and LOGIC +VE outputs are generated relative to the LAMPS -VE and LOGIC -VE lines, which are internally connected together.

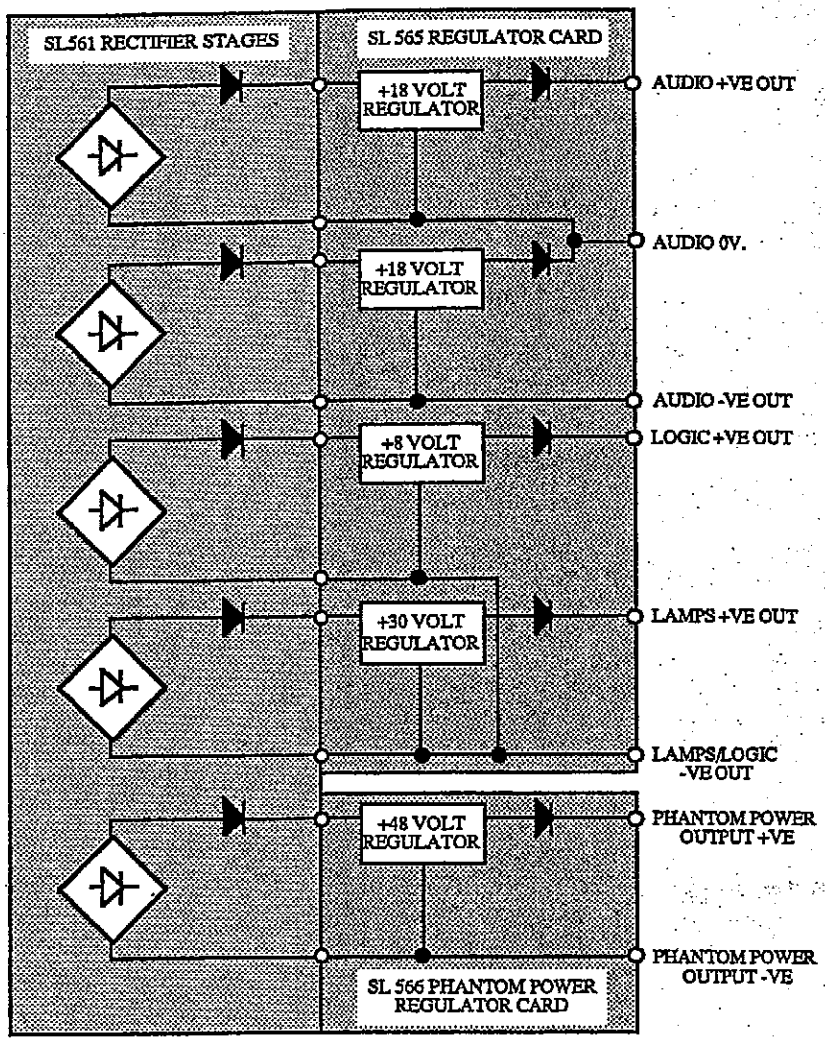


Figure 4. Relationship of Voltage Levels within the SL5000 M Series Power Supply

The unregulated supply lines for the logic, LOGIC + IN and LOGIC - IN, are derived from the SL561. The positive line LOGIC + IN is fed via 5 Amp fuse FS3 to regulator REG3, capacitors C15-16 providing transient filtering on the regulator input. The regulator maintains a constant voltage of approximately 1.25 volts between the O/P and ADJ pins and hence a constant current flows through R19. Virtually the same current (the difference being due to the current flowing from the ADJ pin) flows through RV3 and R20, the output voltage setting network. Bypass capacitor C17 improves ripple rejection, and diodes D18 and D19 provide discharge paths for C18 and C17 respectively, protecting the regulator from damage. Thyristor SCR3 together with R21, R65, C20, and zener diode D22 provide a 'crowbar' circuit to protect the driven load against excessive voltage transients. Note that a link must be fitted in the D21 component position for this feature to operate. The output from REG3 feeds to the output supply bus via a series resistor R22 and a 6 Amp series diode D23. The two test points on the front panel are fed via series resistors R59-60 to prevent inadvertent short-circuiting of the supply, and a yellow front panel indicator LED is driven from the supply via R35.

The unregulated supply lines for the lamps, LAMPS + IN and LAMPS - IN, are similarly derived from the SL561. The positive line LAMPS + IN is fed via 5 Amp fuse FS4 to a pre-regulator consisting of TR3 and surrounding components. This is fitted in order to reduce the power dissipation in the main regulator REG4. Capacitors C15-16 provide transient filtering

on the regulator input. The regulator circuitry is otherwise virtually the same as for the logic supply regulator described above. Bypass capacitor C24 improves ripple rejection, and diodes D25 and D26 provide discharge paths for C26 and C24 respectively, protecting the regulator from damage. Thyristor SCR4 together with R28, R66, C27, and zener diodes D28-29 provide a 'crowbar' circuit to protect the driven load against excessive voltage transients. The output from REG4 feeds to the output supply bus via a series resistor R29 and a 6 Amp series diode D30. The two test points on the front panel are fed via series resistors R61-62 to prevent inadvertent short-circuiting of the supply, and a red front panel indicator LED is driven from the supply via R36. A second regulator, REG5, is driven from the output of REG4 to provide a supply for the fans. This supply is +15 volts with respect to the LAMPS -VE OUT lin, and is fed to the backplane supply bus via 6 Amp series diode D31.

The basic circuitry for the AUDIO + VE and AUDIO - VE regulators is broadly similar to that described above. For the AUDIO + VE side, input is to REG1 via fuse FS1, capacitors C1-2 providing input filtering and bypassing. C4 improves ripple rejection, diodes D3-4 provide discharge paths for C5 and C4 respectively, and the 'crowbar' circuit consists of SCR1, D6-7, C7, R7, and R63. Output to the supply bus is via R8 and D8, the front panel test points are fed via R56-57, and a red front panel LED is driven from the regulated supply via R33. For the AUDIO - VE side, input is to REG2 via fuse FS2, capacitors C8-9 providing input filtering and bypassing. C11 improves ripple rejection, diodes D11-12 provide discharge paths for C12 and C11 respectively, and the 'crowbar' circuit consists of SCR2, D14-15, C14, R16, and R64. Output to the supply bus is via R17 and D16, the front panel test points are fed via R58 and R67, and a green front panel LED is driven from the regulated supply via R34. The 'positive' line of the negative supply feeds via R17 and D16 to the AUDIO 0V line, thus providing a symmetrical balanced supply about this line on the AUDIO + VE and AUDIO - VE lines.

For the AUDIO supplies, additional circuitry is provided to shut down either regulated output if the other line fails. This is accomplished by opto-isolators OPT1-2 together with TR1-2 and associated components. OPT1 controls the AUDIO + VE regulator REG1 via TR1, and OPT2 controls the AUDIO - VE regulator REG2 via TR2. The 'input LEDs' of OPT1 and OPT2 are driven via series resistors R1 and R10 from the AUDIO - VE and AUDIO + VE regulated lines respectively. Under normal operation, both OPT1 and OPT2 are enabled, causing TR1 and TR2 respectively to be switched off.

If the AUDIO + VE line fails, the input LED of OPT2 will be switched off, causing the OPT2 output transistor to turn off and hence TR2 to turn on. This will switch the ADJ pin of REG2 to the AUDIO - VE OUT line, causing this line to rise to within about 1.25 volts of the AUDIO 0V line. This will now turn off the input LED of OPT1. If the AUDIO - VE line fails, the sequence is similar - the input LED of OPT1 will be switched off, causing the OPT1 output transistor to turn off and hence TR1 to turn on. This will switch the ADJ pin of REG1 to the AUDIO 0V line, causing the AUDIO + VE OUT line to fall to within about 1.25 volts of the AUDIO 0V line. This will now turn off the input LED of OPT2.

In either case, the faulty supply must be restored after which both lines will return to the correct voltage.

Circuitry is provided to allow each output to be remotely adjusted (via controls on the front panel of the SL567). For the AUDIO supplies, this circuitry is based around two voltage followers, IC2-3, which are powered from a ±12V supply generated from the AUDIO output lines by regulators REG5-6. Inputs to the voltage follower stages are from AUDIO +VE ADJ. BUS and AUDIO -VE ADJ. BUS for the positive and negative AUDIO outputs respectively. Similar circuitry is used for remote adjustment of the LOGIC and LAMPS outputs, the two voltage follower stages, IC4-5, being powered from a 31.25V supply (relative

to the -25V line) generated by regulator REG7. Inputs to the voltage follower stages are from LOGIC ADJ. BUS and LAMPS ADJ. BUS for the LOGIC and LAMPS outputs respectively.

The four master ADJ. BUS signals are all carried by the SL567 backplane.

OPT3-6 together with comparator IC1 and associated circuitry provide power failure sensing. The outputs of the opto-isolators are connected in series with resistor R45 across the power rails of IC1, and connect to the non-inverting input of IC1 via R46. (This forms the logical equivalent of a 4-input NAND gate connected to IC1, the inputs to the NAND gate being the four regulated supplies.) The inverting input of IC1 is set nominally at 0.6 of the supply voltage by R47-48, and D33-34 constrain the non-inverting input of IC1 to within ±0.7V of the inverting input. Should any of the rectified voltages fail, the relevant opto-isolator OPT3-6 will switch off. This will cause R45-46 to pull the non-inverting input of IC1 high, thus driving the output of IC1 high. Relay RL1 will now be energised, and the piezo sounder in the SL566 Regulator Card will be driven from the output of IC1 via D35, R50, and the Sounder Bus. The 'power available' LED associated with the failed voltage will also extinguish.

2.3 The SL566 Phantom Power Regulator Card (Drawing T85066.71)

The SL566 provides the regulated +48 volt phantom supply used to power capacitor microphones. The unregulated supply lines for the phantom supply are derived from the SL561. The positive line is fed via 0.5 Amp fuse FS1 to regulator REG1, capacitors C1-2 providing transient filtering on the regulator input. The output voltage setting network comprises R1-4 and RV1. Bypass capacitor C3 improves ripple rejection, and diodes D1-2 provide discharge paths for C4 and C3 respectively. Thyristor SCR1 together with R5, R26, C6, and zener diodes D4-5 provide a 'crowbar' circuit to protect the driven load against excessive voltage transients. The output from REG1 feeds to the output supply bus via a series resistor R6 and a 6 Amp series diode D6. The two test points on the front panel are fed via series resistors R7-8 to prevent inadvertent short-circuiting of the supply, and a red front panel indicator LED is driven from the supply via R10-11.

OPT1 together with comparator IC and associated circuitry provide power failure sensing. The output of the opto-isolator is connected in series with resistor R15 across the power rails of IC1, and connect to the non-inverting input of IC1 via R16. The inverting input of IC1 is set nominally at 0.6 of the supply voltage by R17-18, and D7-8 constrain the non-inverting input of IC1 to within ±0.7V of the inverting input. Should the regulated voltage fail, the opto-isolator OPT1 will switch off. This will cause R15-16 to pull the non-inverting input of IC1 high, thus driving the output of IC1 high. The 'FAULT' LED, will now light, relay RL1 will be energised, and the piezo sounder SD1 will provide an audible warning if the associated link is fitted. The 'PHANTOM' LED will also extinguish.

2.4 The SL567 Regulator Rack (Drawings T85067.71, T85167.71-6, T85267.71)

The SL567 Regulator Rack carries the SL565 and SL566 Regulator Cards, and monitors the regulated outputs from the SL565 cards, isolating the supplies from the console if excessive current is drawn from any of the lines. The SL567 can monitor the outputs of up to six SL565 cards. Since each SL565 provides four regulated outputs, the SL567 is thus capable of monitoring 24 supply lines. The lines are monitored in groups of four, as supplied by the SL565 cards. Should any line in such a group draw excessive current, the SL567 de-energises a contactor, thus isolating all four of the lines of that group from the console. A matrix of indicators on the front panel shows immediately which output has been isolated, and hence by implication which bay of the console is drawing excessive current.

The six stages of the SL567 which monitor the power rails from up to six SL565 cards are identical. The circuit description that follows applies to the circuitry monitoring PSU1.

The +18V AUDIO supply passes through a very low value (0.01 Ohms) series resistor, R1, the voltage drop across which is monitored to determine whether excessive current is being drawn by the console. A potential divider on the input side of R1 generates a mid-rail voltage level at the non-inverting input of comparator IC1. A second potential divider on the output side of R1 generates a voltage greater than mid-rail level at the inverting input of IC1 (under normal conditions), due to the offset provided by R17. R9 provides a positive feedback path, and therefore hysteresis, for IC1. The output of IC1 will normally therefore be low, and opto-isolator IC9-A will thus be enabled, causing the SET pin of hybrid circuit H1-A to be pulled low.

Whenever the voltage across R1 increases due to excessive current being drawn by the console, the output of IC1 will switch high, turning off opto-isolator IC9-A. The SET pin of H1-A is hence pulled high, causing the output of H1-A to latch high. This line drives the front panel 'fault' LED on via TR1 (Drawing T85267.71) turns TR1 (Drawing T85167.71) off via IC19-A, thus de-energising the contactor, and resets latches H1-B, H2-A, and H2-B via IC10-B, IC11-A, and IC11-B respectively. The de-energising of the contactor isolates the faulty console bay from the power supply. The bay will remain isolated until the RESET button is pressed. In either case, if the fault remains the console bay will once again be isolated from the supply as soon after completion of the reset sequence as it takes for the circuitry to again detect the excessive current demand from the console bay at fault. Typically, this would be perhaps a millisecond or two to detect the fault and another fifteen to twenty milliseconds for the contactor to condescend to drop out !!

Whilst the low-value series sensing resistor values (and those of the potential dividers on the comparator inputs) may differ in value for the other three circuits, in all other respects the circuitry is virtually identical. Any of the four latches may be reset by any of the other three latches, and each latch output can turn on the relevant front panel 'fault' LED via TR2-4 (Drawing T85267.71) and turn off TR1 (Drawing T85167.71) via IC9-A and a 4-input OR gate composed of D1-4. In addition, all four latches can be reset by means of the RESET line, generated at the output of IC13-A either from the front panel pushbutton via TR2 (Drawing T85167.71) and D5 or via opto-isolator IC12 from the MO257 connector. Provision is made via link 1 for the RESET line to be asserted on power-up by a signal from power supply monitor IC15 driving TR2 (Drawing T85167.71) via IC13-B, IC13-C and D6.

A 24V d.c. supply for the contactor is supplied by transformer T1, rectifier BR1, regulator IC51, and associated components. The 6V d.c. power for the front panel indicators and the logic is derived from this 24V supply by regulator IC14 and associated components.

The Battery Backup circuitry consists of regulators IC32-33, comparators IC34 and IC53, and associated circuitry (Drawing T85167.73). The circuit is fed from the LAMPS supply. This is first regulated to around 17V by IC32. IC32 acts as a pre-regulator, and is fitted in order to reduce the power dissipation in the main regulator IC33.

The output from IC32 passes through a low value (1 Ohm) series resistor, R143, the voltage drop across which is monitored by a comparator circuit based around IC53. If the battery is being charged, current through R143 (and hence the voltage across it) will increase, lowering the voltage at the inverting input of IC53. When this voltage reaches the level of the reference voltage at pin 2 of IC53, the output of IC53 will switch HIGH, turning on the front panel CHARGE indicator, D29.

The main regulator, IC33, is fed from R143 via diode D29, which prevents any leakage from the battery back through the pre-regulator circuitry. The regulated 6.82V output of IC33 charges the battery directly. Zener diode D32 protects the battery against over-voltage. The battery output passes to the console via a 5A fuse and two diodes, D30-31. This ensures that no current is supplied to the console by the battery unless power failure has occurred.

Comparator IC34 monitors the battery voltage and lights the front panel LO BATT indicator, D34, if either the battery output falls below 5.5V or the fuse blows.

2.5 The Power Distribution/Fan Driver Monitor Cards (Drawing T85263.71)

This card handles the referencing and distribution of the supply lines within the console, and can also drive and monitor up to two fans.

The -25V, 0V AUDIO, and Battery lines are daisy-chained through the console via the distribution cards. All of the supply lines are floating with respect to each other as they arrive at the distribution cards, where the AUDIO supplies are referenced to the LOGIC supplies. The referencing is performed by a Schottky diode, D4, which links the LOGIC +VE line to the AUDIO -VE line. (Direct linking cannot be used because, if the AUDIO supplies cut out, the LOGIC +VE line would adopt the level of the AUDIO 0V line due to the low impedance presented by the analogue circuitry, and thus present an excessively high voltage supply to the logic circuitry.) Resistor R1 forward biases D4, thus the LOGIC +VE line is held at around -17.7 volts relative to the AUDIO 0V line.

The LOGIC +VE line from the contactors drives the -18V BACKUP line via Schottky diode D2. This line is the positive supply for all console logic . The -18V BACKUP line is also fed from the BATTERY -18V line, Schottky diode D5 matching the voltage drop of D2. Diode D6 protects the logic against inter-rail short circuits reverse-biasing (and hence destroying) the logic circuitry.

The distribution board also contains the fan driving and failure detection circuitry, two identical circuits being incorporated. The circuit is designed to operate with brushless d.c. motor fans which generate four 'current pulses' per revolution. These are converted into voltage pulses which are used to confirm that the fan is operating correctly.

Supply to the fan connector MO 199 is via R5 and TR2, whilst D9 provides visible indication of operation. The current pulses from the fan are converted into voltage pulse by R6, and then fed via C6 into IC4-A. This converts the fan pulses to CMOS-compatible levels. The pulses output from IC4-A are fed to binary counter IC5-A, which produces an output on every fourth such pulse. The output from counter IC5-A triggers a monostable, IC1-A.

The positive output pulse from IC1-A clears the counter IC5-A to zero, whilst the negative output pulse triggers a second monostable, IC1-B. This monostable has a period of some 5 seconds, and is re-triggerable. The same output also causes the fan supply to be interrupted by turning off TR2 for the duration of the pulse. Under normal operation of the fan, the above process repeats forever, monostable IC1-B always being re-triggered by IC1-A. Should the fan stop, IC1-B will not be re-triggered and the output will go high. This will turn on TR5, activating the Fan Warning Bus, and will also enable a gated oscillator consisting of IC3 and associated components. The oscillator output switches TR1, which turns off TR2, and hence the fan supply.

This resets the internal "locked rotor protection" circuitry of the fan before power is re-applied in an attempt to restart it. This process repeats until either the fan starts or power is removed.

4. Connector Details

This section provides a pin-by-pin guide to the signal and cabling details for each of the main connectors within the power supply system.

4.1 SL561 Transformer and Rectifier Unit Output Connectors

Connector Name: DIN65
Location: Rear Panel of SL561 Transformer and Rectifier Unit (Two off)
Rear Panel of SL567 Racks
Connector Type: DIN 41612 'F' Type - 96-way

1b	n/c	1d	n/c	1z	n/c
2b	+ ve AUDIO +	2d	+ ve AUDIO +	2z	+ ve AUDIO +
3b	n/c	3d	n/c	3z	n/c
4b	+ ve AUDIO +	4d	+ ve AUDIO +	4z	+ ve AUDIO +
5b	n/c	5d	n/c	5z	n/c
6b	+ ve AUDIO -	6d	+ ve AUDIO -	6z	+ ve AUDIO -
7b	n/c	7d	n/c	7z	n/c
8b	+ ve AUDIO -	8d	+ ve AUDIO -	8z	+ ve AUDIO -
9b	n/c	9d	n/c	9z	n/c
10b	- ve AUDIO +	10d	- ve AUDIO +	10z	- ve AUDIO +
11b	n/c	11d	n/c	11z	n/c
12b	- ve AUDIO +	12d	- ve AUDIO +	12z	- ve AUDIO +
13b	n/c	13d	n/c	13z	n/c
14b	- ve AUDIO -	14d	- ve AUDIO -	14z	- ve AUDIO -
15b	n/c	15d	n/c	15z	n/c
16b	- ve AUDIO -	16d	- ve AUDIO -	16z	- ve AUDIO -
17b	n/c	17d	n/c	17z	n/c
18b	LOGIC +	18d	LOGIC +	18z	LOGIC +
19b	n/c	19d	n/c	19z	n/c
20b	LOGIC +	20d	LOGIC +	20z	LOGIC +
21b	n/c	21d	n/c	21z	n/c
22b	LOGIC -	22d	LOGIC -	22z	LOGIC -
23b	n/c	23d	n/c	23z	n/c
24b	LOGIC -	24d	LOGIC -	24z	LOGIC -
25b	n/c	25d	n/c	25z	n/c
26b	LAMPS +	26d	LAMPS +	26z	LAMPS +
27b	n/c	27d	n/c	27z	n/c
28b	LAMPS -	28d	LAMPS -	28z	LAMPS +
29b	n/c	29d	n/c	29z	n/c
30b	LAMPS -	30d	PHANTOM +	30z	LAMPS -
31b	n/c	31d	n/c	31z	n/c
32b	P/F Relay Contact 'A'	32d	P/F Relay Contact 'B'	32z	PHANTOM -

4.2 Power Supply Connections to Console

Connector Name: 1A-B, 2A-B, 3A-B, 4A-B, 5A-B, 6A-B
Location: Rear Panel of SL567: Twelve connectors (Six pairs)
Connector Type: 19-way BICC

Pin	Description	Cable	Colour
A	+18V 5A Audio	32/0.2	Red
B	+18V 5A Audio	32/0.2	Red
C	- 18V 5A Logic/LEDs	32/0.2	White
D	- 18V 5A Logic/LEDs	32/0.2	White
E	- 18V 5A Logic/LEDs	32/0.2	White
F	+ 5V 2A Lamps	32/0.2	Pink
G	-25V 5A Logic/LEDs	32/0.2	Brown
H	-25V 2A Lamps	32/0.2	Purple
J	0V 5A Audio	32/0.2	Green
K	0V 5A Audio	32/0.2	Green
L	not used		
M	not used		
N	-18V 5A Audio	32/0.2	Blue
P	FAN + ve	16/0.2	Blue
R	-18V 5A Audio	32/0.2	Blue
S	-25V 5A Logic/LEDs	32/0.2	Brown
T	-25V 5A Logic/LEDs	32/0.2	Brown
U	FAN - ve	16/0.2	White
V	GROUND (Fit Link LK1 to connect to 0V Audio at pins J and K)		
Z	not used		

4.3 Battery Backup Connection to Console

Connector Identification: 'BATTERY BACKUP OUTPUT'
Location: Rear Panel of SL567
Connector Type: 8-way BICC

Pin	Description	Cable	Colour
A	-18V BACKUP	32/0.2	White
B	FAN WARNING	32/0.2	Black
C	- 24V BACKUP	32/0.2	Brown
D	not used		
E	not used		
F	not used		
G	not used		
H	FAN WARNING +	32/0.2	Red

4.4 Fault Relay Output from Power Supply Rack

Connector Identification: 'Fault Relay Contacts'
Location: Rear Panel of SL567
Connector Type: 8-way BICC

Pin	Description	Cable	Colour
A	Power Fail Relay	16/0.2	Black
B	Power Fail Relay	16/0.2	White
C	not used		
D	not used		
E	not used		
F	not used		
G	not used		
H	not used		

4.5 Power Supply Rack Parallel Connectors

Connector Identification: 'PSU RACK PARALLEL'
Location: Rear Panel of SL567 (Two off)
Connector Type: 19-way BICC

Pin	Description	Cable	Colour
A	AUDIO + ve	32/0.2	Red
B	AUDIO + ve	32/0.2	Red
C	LOGIC + ve	32/0.2	White
D	LOGIC + ve	32/0.2	White
E	LOGIC + ve	32/0.2	White
F	LAMPS + ve	32/0.2	Pink
G	LOGIC - ve	32/0.2	Brown
H	LAMPS - ve	32/0.2	Purple
J	AUDIO 0V	32/0.2	Green
K	AUDIO 0V	32/0.2	Green
L	not used		
M	not used		
N	AUDIO - ve	32/0.2	Blue
P	not used		
R	AUDIO - ve	32/0.2	Blue
S	LOGIC - ve	32/0.2	Brown
T	LOGIC - ve	32/0.2	Brown
U	not used		
V	not used		

4.6 Phantom Power Output to Console

Connector Identification: '48V Phantom Power Output'
Location: Rear Panel of SL567
Connector Type: 4-way BICC

Pin	Description	Cable	Colour
A	Phantom Power + ve	32/0.2	Orange
B	not used		
C	Phantom Power - ve	32/0.2	Black
D	not used		

4.7 External D.C. Input Connector

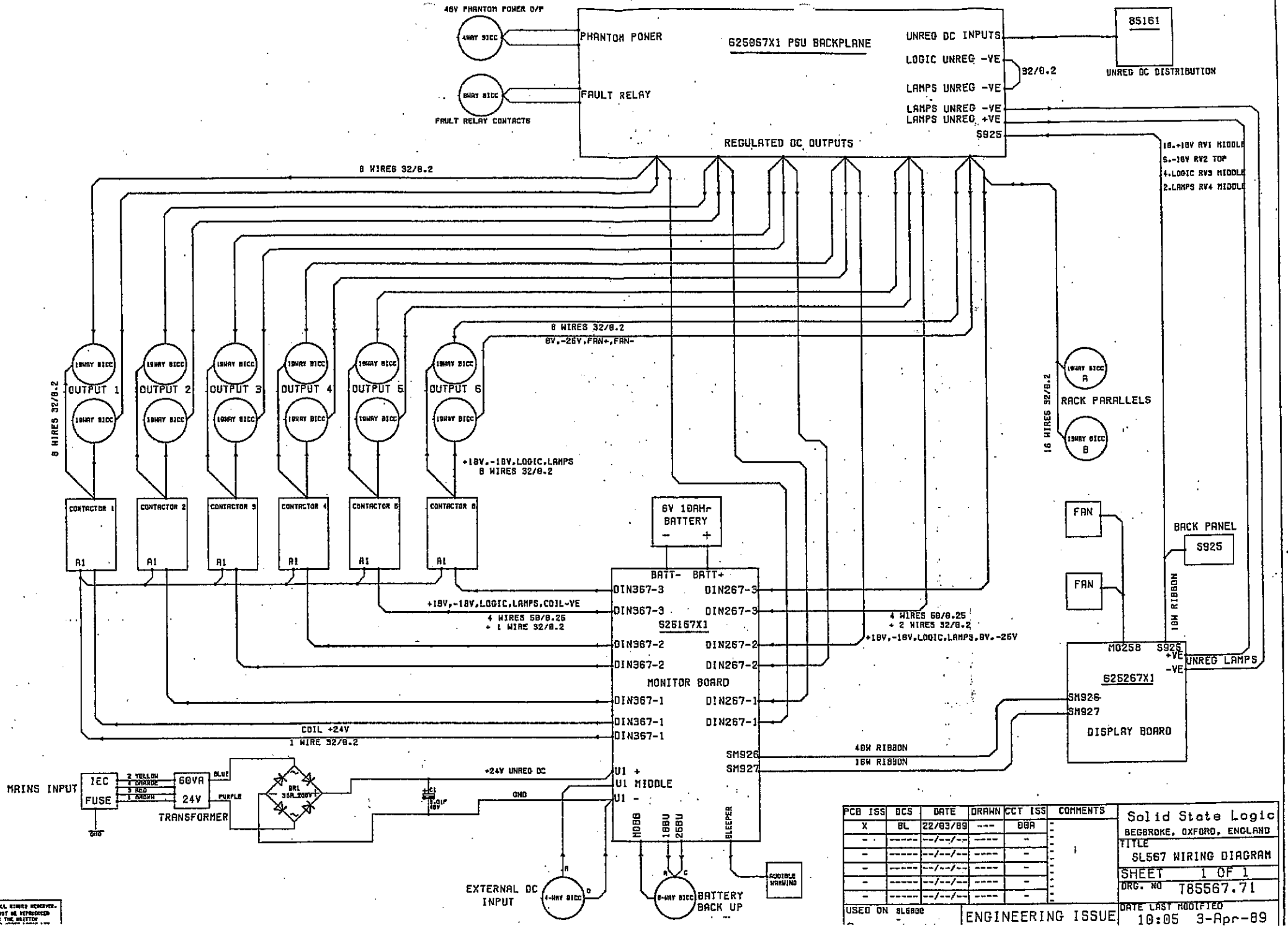
Connector Identification: 'EXTERNAL D.C. INPUT'
Location: Rear of SL567
Connector Type: 4-way BICC

Pin	Description	Cable	Colour
A	Voltage + ve	32/0.2	Red
B	not used		
C	not used		
D	Voltage - ve	32/0.2	Black

4.8 Power Connectors within the console

Connector Name: MO60
Location: From Power Distribution Board to points throughout console
Connector Type: 8-way Molex ribbon connector

Pin	Description	Colour
1	Lamps + ve	Brown
2	+ 18V	Red
3	0V	Orange
4	0V	Yellow
5	- 18V	Green
6	-18V Battery Backup	Blue
7	- 24V	Purple
8	-18V Logic	Grey



PCB ISS	DCS	DATE	DRAWN	CCT ISS	COMMENTS
X	BL	22/03/89	---	00A	
-	------	--/--/--	-----	-	
-	------	--/--/--	-----	-	
-	------	--/--/--	-----	-	
-	------	--/--/--	-----	-	
-	------	--/--/--	-----	-	

USED ON SL6000

ENGINEERING ISSUE

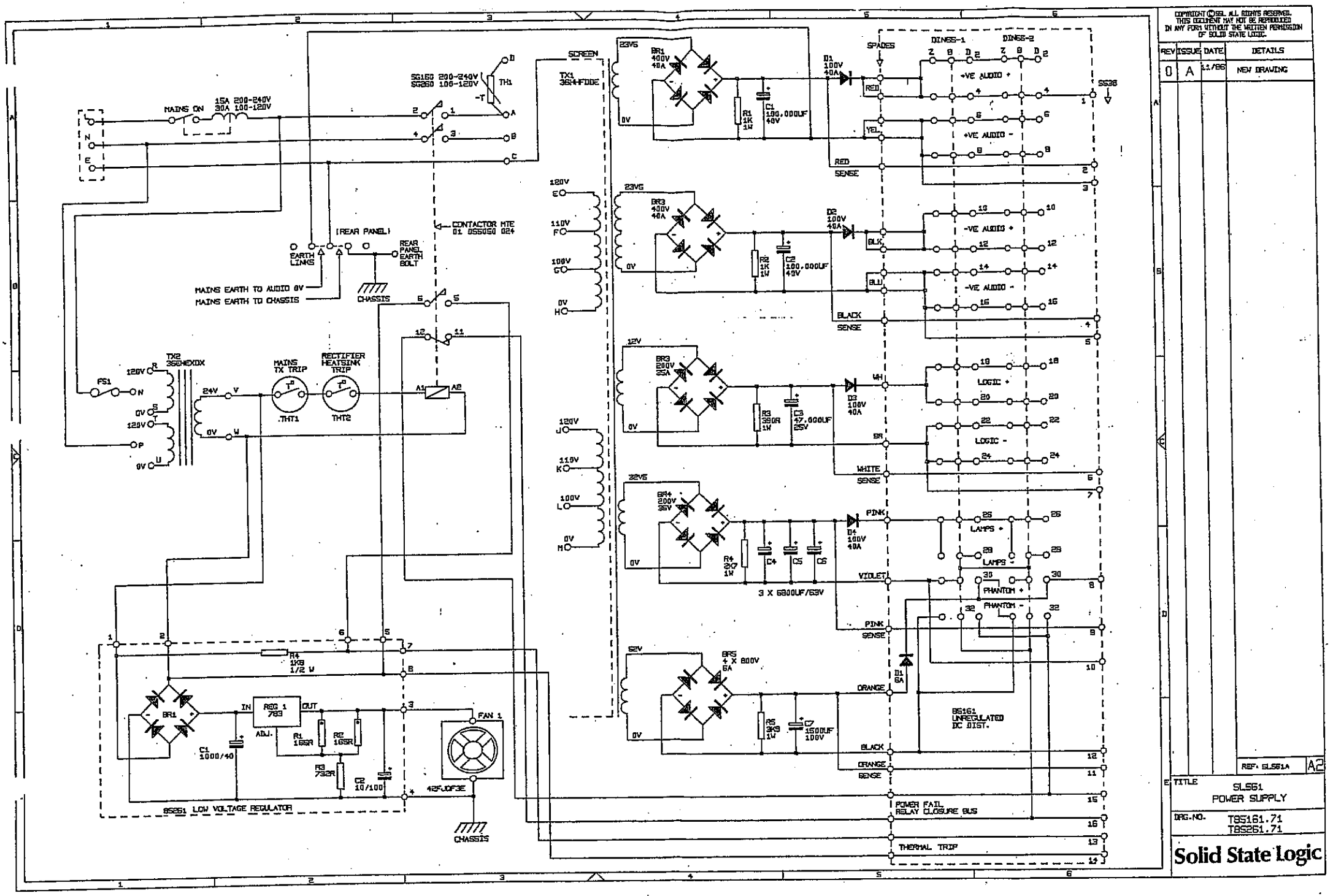
Solid State Logic
BEGBROKE, OXFORD, ENGLAND

TITLE
SL567 WIRING DIAGRAM

SHEET 1 OF 1

DRG. NO T85567.71

DATE LAST MODIFIED
10:05 3-Apr-89



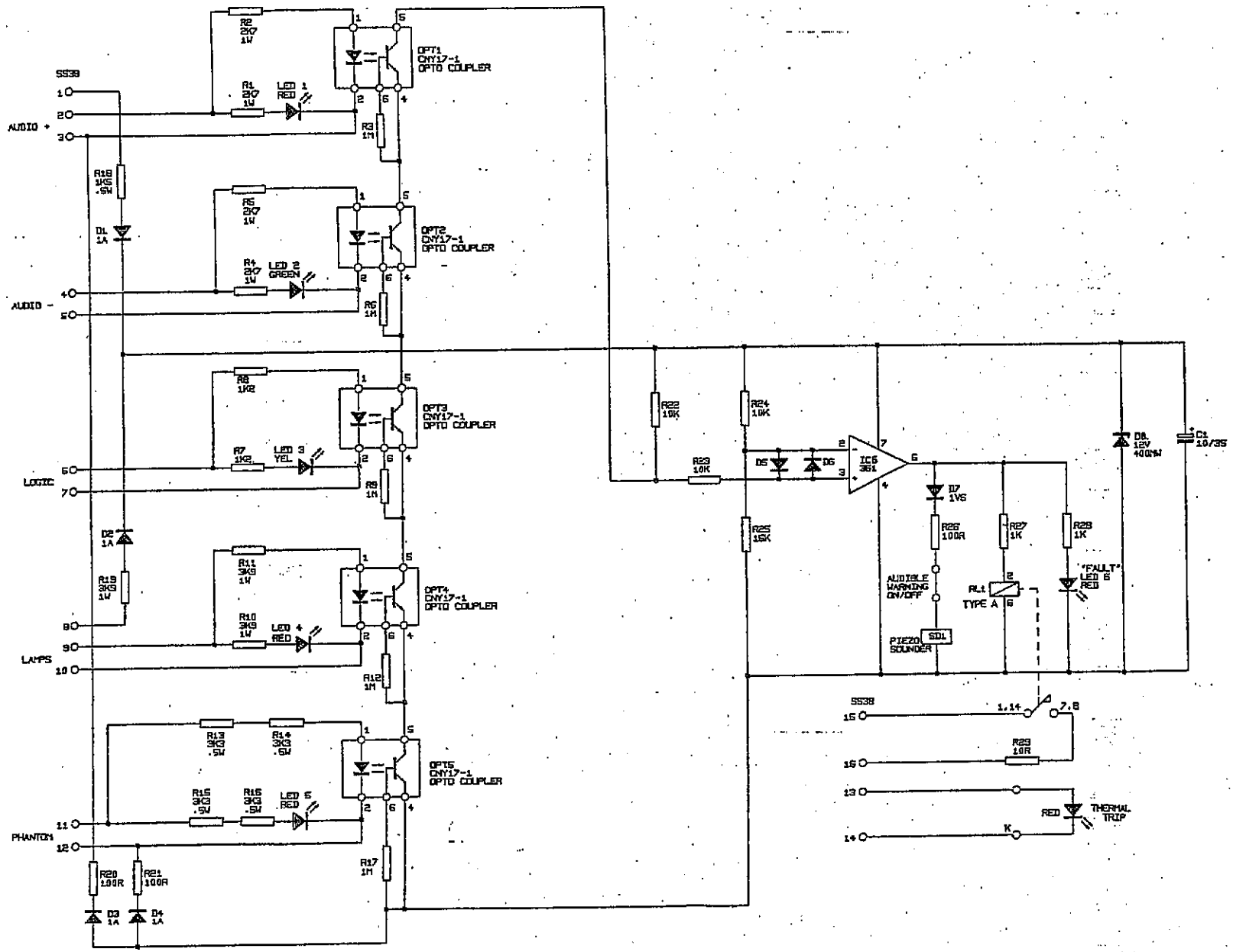
REV	ISSUE	DATE	DETAILS
0	A	11/86	NEW DRAWING

REF: SLS61A A2

TITLE
SLS61
POWER SUPPLY

DRG.NO. T85161.71
T85261.71

Solid State Logic



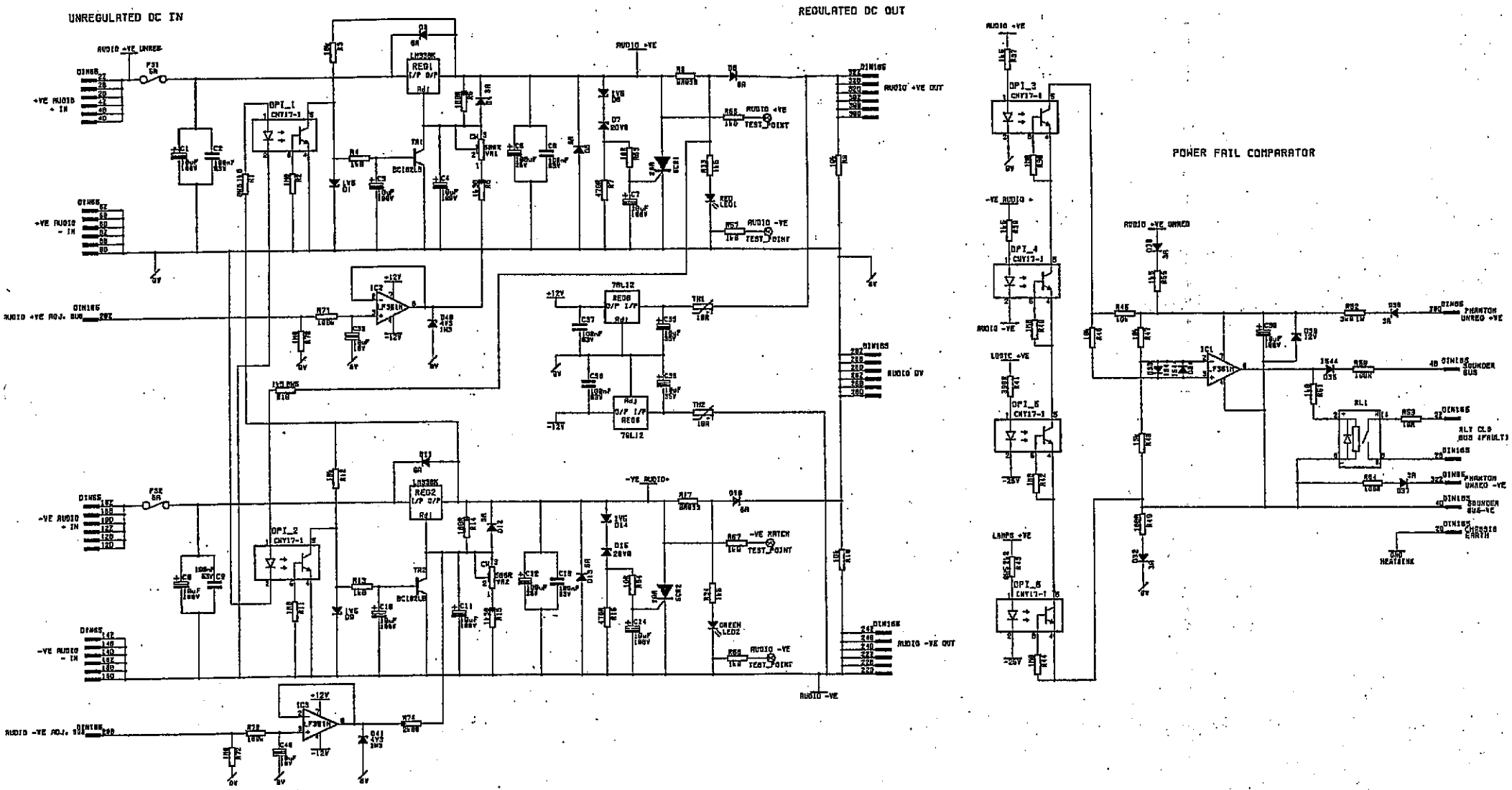
REV	ISSUE	DATE	DETAILS
0	A	12/86 JE	NEW DRAWING
0	B	3/87 JE	LED 4 WAS YEL
0	C	3/87 BC	IC6 WAS IC1 D8 WAS ZD1

REF: SL5618 A2

TITLE: SL561 P/S CARD & POWER FAIL SENSE

DRG.NO. T85061.71

Solid State Logic



PCB ISS	DCS	DATE	DRAWN	CCT ISS	COMMENTS
JK	BC	19/01/88	MC	88x	APROVED 11/88
-	------	--/--/--	----	-	
-	------	--/--/--	----	-	
-	------	--/--/--	----	-	
-	------	--/--/--	----	-	
-	------	--/--/--	----	-	

USED ON SL665 X3

ENGINEERING ISSUE

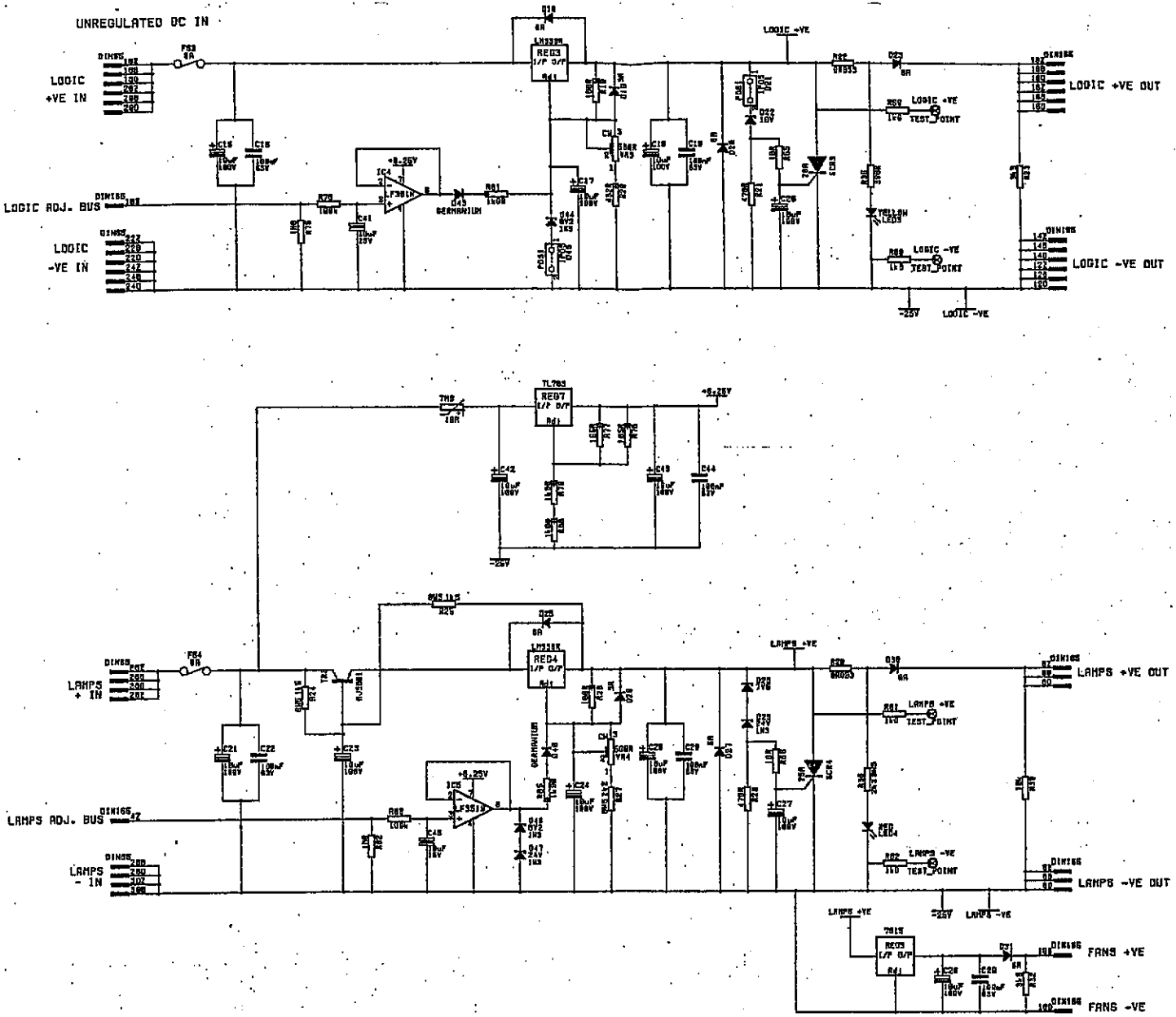
Solid State Logic
BEGBROKE, OXFORD, ENGLAND

TITLE
SL665 REGULATOR CARD

SHEET 1 OF 2

DRG. NO
885065.71

DATE LAST MODIFIED
10:47 29-Nov-88



PCB ISS	DCS	DATE	DRAWN	CCT ISS	COMMENTS
JK	BC	19/01/88	MC	88x	APPROVED 11/88
-	------	--/--/--	----	-	
-	------	--/--/--	----	-	
-	------	--/--/--	----	-	
-	------	--/--/--	----	-	
-	------	--/--/--	----	-	
USED ON SL565 X3		ENGINEERING ISSUE			

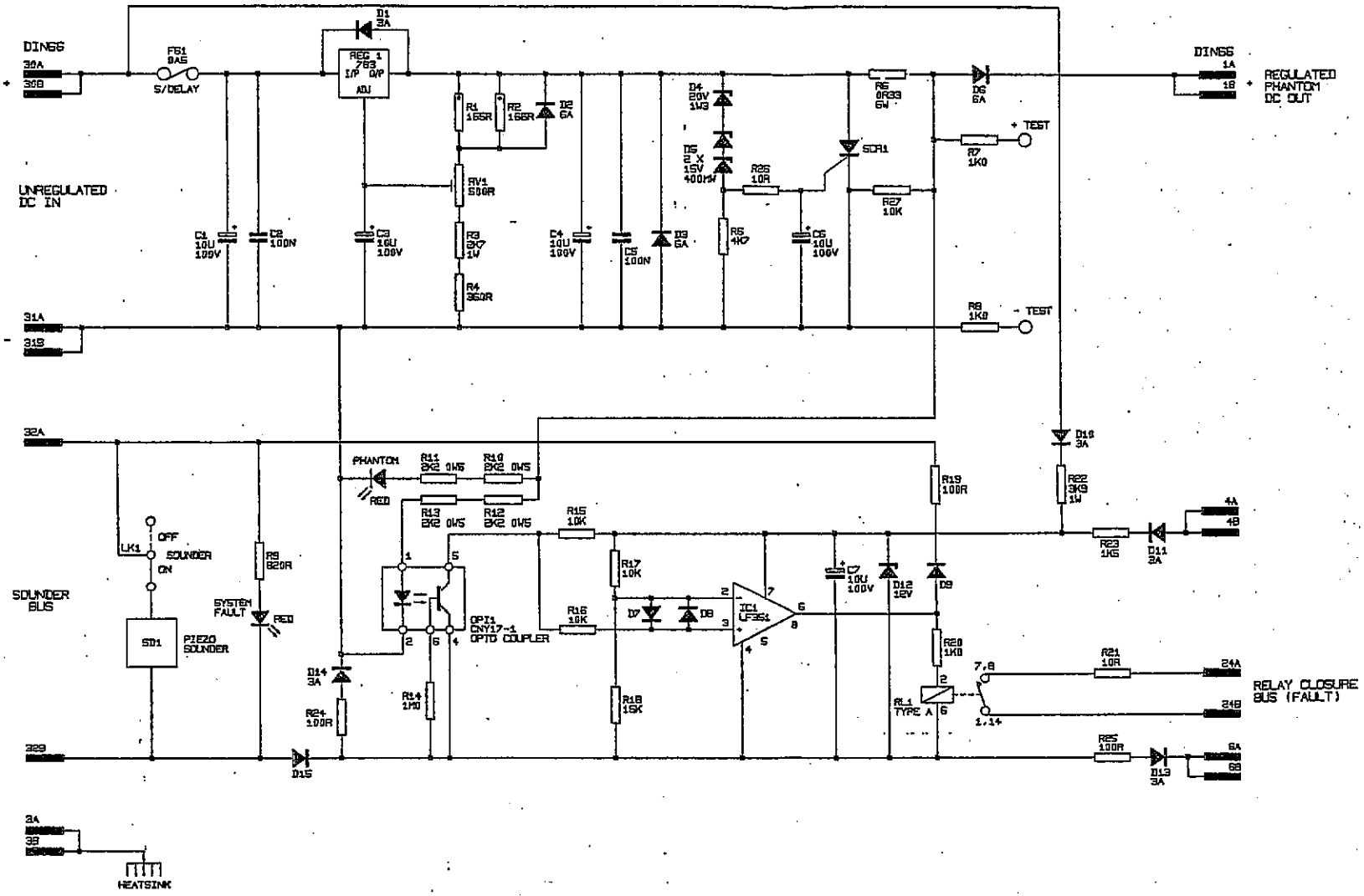
Solid State Logic
BEGBROKE, OXFORD, ENGLAND

TITLE
SL565 REGULATOR CARD

SHEET 2 OF 2

DRG. NO
s85065.72

DATE LAST MODIFIED
11:07 29-Nov-88



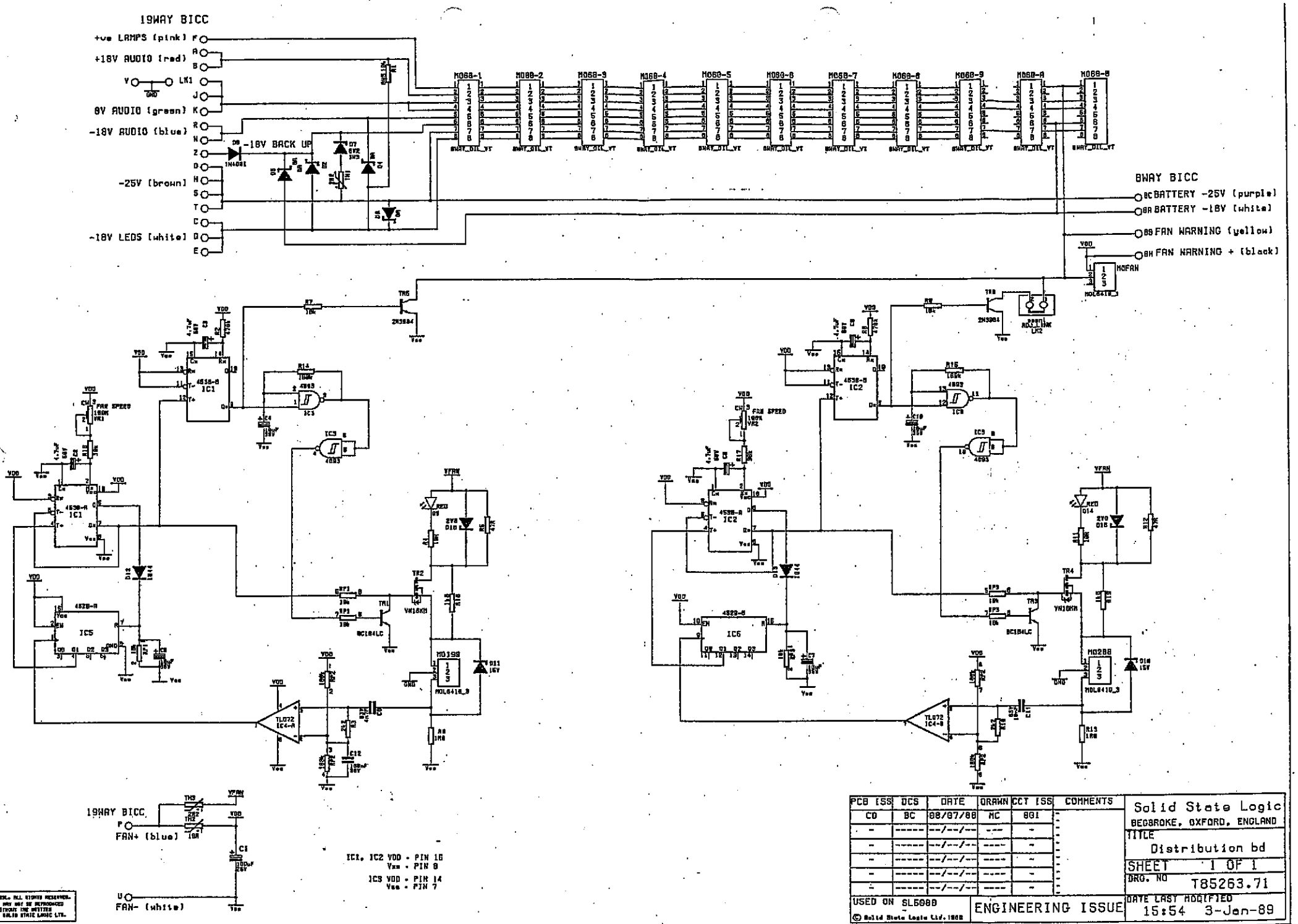
REV	ISSUE	DATE	DETAILS
0	A	JE FEB 87	NEW DRAWING STEFF
0	B	JE APR 87	R4 WAS 430R NOW 360R STEFF
0	C	JE APR 87	D5 WAS 33V NOW 2 X 15V, R5 WAS 470R NOW 4K7 D14 & R24 POSITION ALTERED STEFF

REF: SL566A A2

TITLE
SL566
PHANTOM REGULATOR

DRG. NO. T85066.71

Solid State Logic



PCB ISS	DCS	DATE	DRAWN	CCT ISS	COMMENTS
CD	BC	08/07/88	MC	801	
-	------	--/--/--	---	-	
-	------	--/--/--	----	-	
-	------	--/--/--	-----	-	
-	------	--/--/--	-----	-	
-	------	--/--/--	-----	-	

USED ON SL5080

ENGINEERING ISSUE

Solid State Logic
BEGBROKE, OXFORD, ENGLAND

TITLE
Distribution bd

SHEET 1 OF 1

DRG. NO T85263.71

DATE LAST MODIFIED
15:54 3-Jan-89